

24-Bit, 192-kHz Sampling, Enhanced Multi-Level, $\Delta\Sigma$, Eight-Channel, Audio Digital-to-Analog Converter

FEATURES

- **24-Bit, 8-Channel, Delta-Sigma DAC:**
 - High Performance (Single-Ended, $f_s = 48$ kHz)
 - THD+N: -94 dB
 - SNR: 111 dB
 - Dynamic Range: 111 dB
 - Sampling Rate: 8 kHz to 192 kHz
 - System Clock: 128 f_s , 192 f_s , 256 f_s , 384 f_s , 512 f_s , 768 f_s , 1152 f_s
 - Single-Ended Voltage Output: 4 V_{PP}
 - Analog Low-Pass Filter Included
 - 4x/8x Oversampling Digital Filter:
 - Passband Ripple: ± 0.0018 dB
 - Stop Band Attenuation: -75 dB
 - Zero Flags (16-/20-/24-Bits)
- **Flexible Audio Interface:**
 - I/F Format:
 - I²S™, Left-/Right-Justified, DSP, TDM
 - Data Length: 16, 20, 24, 32 Bits
- **Flexible Mode Control:**
 - 3-Wire SPI™, 2-Wire I²C™-Compatible Serial Control Interface, or Hardware Control
- **Multi Functions via SPI or I²C I/F:**
 - Audio I/F Format Select: I²S, Left-Justified, Right-Justified, DSP, TDM
 - Digital Attenuation and Soft Mute
 - Digital De-Emphasis:
 - 32 kHz, 44.1 kHz, 48 kHz
 - Data Polarity Control
 - Power-Down
- **Multi Functions via Hardware Control:**
 - Audio I/F Format Select: I²S, TDM
 - Digital De-Emphasis Filter: 44.1 kHz

- **Analog Mute by Clock Halt Detection**
- **External Reset Pin**
- **Power Supplies:**
 - 5-V Analog
 - 3.3-V Digital
- **Package: HTSSOP-48**
- **Operating Temperature Range:**
 - -40°C to $+85^{\circ}\text{C}$

APPLICATIONS

- Blu-ray Disc™ Players
- DVD Players
- AV Receivers
- Home Theaters
- Car Audio External Amplifiers
- Car Audio AVN Applications

DESCRIPTION

The PCM1691 is a high-performance, single-chip, 24-bit, eight-channel, audio digital-to-analog converter (DAC) with single-ended outputs. The eight-channel, 24-bit DAC employs an enhanced multi-level, delta-sigma ($\Delta\Sigma$) modulator, and supports 8-kHz to 192-kHz sampling rates and a 16-/20-/24-/32-bit width digital audio input word on the audio interface. The PCM1691 audio interface supports a time-division-multiplexed (TDM) format in addition to I²S, left-justified, right-justified, and DSP formats.

The PCM1691 can be controlled through a three-wire, SPI-compatible or two-wire, I²C-compatible serial interface in software, which provides access to all functions including digital attenuation, soft mute, de-emphasis, and so forth. Additionally, hardware control mode provides two user-programmable functions through two control pins. The PCM1691 is available in a 12-mm \times 8-mm (12-mm \times 6-mm body), 48-pin HTSSOP package.



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SPI is a trademark of Motorola, Inc.

I²S, I²C are trademarks of NXP Semiconductors.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---------|--------------|--------------------|-----------------------------|-----------------|-----------------|---------------------------|
| PCM1691 | HTSSOP-48 | DCA | –40°C to +85°C | PCM1691 | PCM1691DCA | Tube, 40 |
| | | | | | PCM1691DCAR | Tape and Reel, 2000 |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | PCM1691 | UNIT |
|--|---|----------------------------|------|
| Supply voltage | VCC1, VCC2 | –0.3 to +6.5 | V |
| | VDD | –0.3 to +4.0 | V |
| Ground voltage differences: AGND1, AGND2, DGND | | ±0.1 | V |
| Supply voltage differences: VCC1, VCC2 | | ±0.1 | V |
| Digital input voltage | RST, TEST, MS, MC, MD, SCKI, AMUTEI, AMUTEO | –0.3 to +6.5 | V |
| | BCK, LRCK, DIN1/2/3/4, MODE, ZERO1, ZERO2 | –0.3 to (VDD + 0.3) < +4.0 | V |
| Analog input voltage: VCOM, VOUT1–8 | | –0.3 to (VCC + 0.3) < +6.5 | V |
| Input current (all pins except supplies) | | ±10 | mA |
| Ambient temperature under bias | | –40 to +125 | °C |
| Storage temperature | | –55 to +150 | °C |
| Junction temperature | | +150 | °C |
| Lead temperature (soldering, 5s) | | +260 | °C |
| Package temperature (IR reflow, peak) | | +260 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | PCM1691 | | | UNIT |
|---|------------------------------|-------------------|-----|--------|-----------------|
| | | MIN | TYP | MAX | |
| Analog supply voltage, VCC | | 4.5 | 5.0 | 5.5 | V |
| Digital supply voltage, VDD | | 3.0 | 3.3 | 3.6 | V |
| Digital interface | | LVTTTL-compatible | | | |
| Digital input clock frequency | Sampling frequency, LRCK | 8 | | 192 | kHz |
| | System clock frequency, SCKI | 2.048 | | 36.864 | MHz |
| Analog output voltage | Single-ended | | 4 | | V _{PP} |
| Analog output load resistance to ac-coupled GND | | 5 | | | kΩ |
| Analog output load capacitance | | | | 50 | pF |
| Digital output load capacitance | | | | 20 | pF |
| Operating free-air temperature | PCM1691 consumer grade | –40 | +25 | +85 | °C |

ELECTRICAL CHARACTERISTICS: Digital Input/Output

All specifications at $T_A = +25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $SCKI = 512 f_S$, 24-bit data, and Sampling mode = Auto, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | PCM1691 | | | UNIT |
|---|---|------------------------------------|----------------------|----------|---------------|
| | | MIN | TYP | MAX | |
| DATA FORMAT | | | | | |
| Audio data interface format | | I ² S, LJ, RJ, DSP, TDM | | | |
| Audio data word length | | 16, 20, 24, 32 | | | Bits |
| Audio data format | | MSB first, twos complement | | | |
| Sampling frequency | f_S | 8 | 48 | 192 | kHz |
| System clock frequency | 128 f_S , 192 f_S , 256 f_S , 384 f_S , 512 f_S , 768 f_S , 1152 f_S | 2.048 | | 36.864 | MHz |
| INPUT LOGIC | | | | | |
| Input logic level | $V_{IH}^{(1)(2)}$ | 2.0 | | VDD | VDC |
| | $V_{IL}^{(1)(2)}$ | | | 0.8 | VDC |
| Input logic level | $V_{IH}^{(3)(4)}$ | 2.0 | | 5.5 | VDC |
| | $V_{IL}^{(3)(4)}$ | | | 0.8 | VDC |
| Input logic current | $I_{IH}^{(2)(3)}$ | $V_{IN} = V_{DD}$ | | ± 10 | μA |
| | $I_{IL}^{(2)(3)}$ | $V_{IN} = 0\text{ V}$ | | ± 10 | μA |
| Input logic current | $I_{IH}^{(1)(4)}$ | $V_{IN} = V_{DD}$ | +65 | +100 | μA |
| | $I_{IL}^{(1)(4)}$ | $V_{IN} = 0\text{ V}$ | | ± 10 | μA |
| OUTPUT LOGIC | | | | | |
| Output logic level | $V_{OH}^{(5)}$ | $I_{OUT} = -4\text{ mA}$ | 2.4 | | VDC |
| | $V_{OL}^{(5)(6)}$ | $I_{OUT} = +4\text{ mA}$ | | 0.4 | VDC |
| REFERENCE OUTPUT | | | | | |
| VCOM output voltage | | | $0.5 \times V_{CC1}$ | | V |
| VCOM output impedance | | | 7.5 | | k Ω |
| Allowable VCOM output source/sink current | | | | 1 | μA |

- (1) BCK and LRCK (Schmitt trigger input with 50-k Ω typical internal pull-down resistor).
- (2) DIN1/2/3/4 (Schmitt trigger input).
- (3) SCKI, TEST/ADR1/RSV, MC/SCL/FMT, MD/SDA/DEMP, and AMUTEI (Schmitt trigger input, 5-V tolerant).
- (4) RST and MS/ADR0/RSV (Schmitt trigger input with 50-k Ω typical internal pull-down resistor, 5-V tolerant).
- (5) ZERO1 and ZERO2.
- (6) SDA (I²C mode, open-drain low output), and AMUTE0 (open-drain low output).

ELECTRICAL CHARACTERISTICS: DAC

All specifications at $T_A = +25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $SCKI = 512 f_S$, 24-bit data, and Sampling mode = Auto, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | PCM1691 | | | UNIT | |
|--|---|---|------------------------|--------------------|------------|----|
| | | MIN | TYP | MAX | | |
| RESOLUTION | | 16 | 24 | | Bits | |
| DC ACCURACY | | | | | | |
| Gain mismatch channel-to-channel | | | ± 2.0 | ± 6.0 | % of FSR | |
| Gain error | | | ± 2.0 | ± 6.0 | % of FSR | |
| Bipolar zero error | | | ± 1.0 | | % of FSR | |
| DYNAMIC PERFORMANCE⁽¹⁾⁽²⁾ | | | | | | |
| Total harmonic distortion + noise | THD+N | $V_{OUT} = 0\text{ dB}$ | $f_S = 48\text{ kHz}$ | -94 | -86 | dB |
| | | | $f_S = 96\text{ kHz}$ | -94 | | dB |
| | | | $f_S = 192\text{ kHz}$ | -94 | | dB |
| Dynamic range | | $f_S = 48\text{ kHz}$, EIAJ, A-weighted | 104 | 111 | | dB |
| | | $f_S = 96\text{ kHz}$, EIAJ, A-weighted | | 111 | | dB |
| | | $f_S = 192\text{ kHz}$, EIAJ, A-weighted | | 111 | | dB |
| Signal-to-noise ratio | SNR | $f_S = 48\text{ kHz}$, EIAJ, A-weighted | 104 | 111 | | dB |
| | | $f_S = 96\text{ kHz}$, EIAJ, A-weighted | | 111 | | dB |
| | | $f_S = 192\text{ kHz}$, EIAJ, A-weighted | | 111 | | dB |
| Channel separation (between one channel and others) | | $f_S = 48\text{ kHz}$ | 100 | 106 | | dB |
| | | $f_S = 96\text{ kHz}$ | | 106 | | dB |
| | | $f_S = 192\text{ kHz}$ | | 105 | | dB |
| ANALOG OUTPUT | | | | | | |
| Output voltage | Single-ended | | $0.8 \times V_{CC1}$ | | V_{PP} | |
| Center voltage | | | $0.5 \times V_{CC1}$ | | V | |
| Load impedance | To ac-coupled GND | 5 | | | k Ω | |
| LPF frequency response | $f = 20\text{ kHz}$ | | -0.04 | | dB | |
| | $f = 44\text{ kHz}$ | | -0.18 | | dB | |
| DIGITAL FILTER PERFORMANCE WITH SHARP ROLL-OFF | | | | | | |
| Passband (single, dual) | Except $SCKI = 128 f_S$ and $192 f_S$ | | | $0.454 \times f_S$ | Hz | |
| | $SCKI = 128 f_S$ and $192 f_S$ | | | $0.432 \times f_S$ | Hz | |
| Passband (quad) | | | | $0.432 \times f_S$ | Hz | |
| Stop band (single, dual) | Except $SCKI = 128 f_S$ and $192 f_S$ | $0.546 \times f_S$ | | | Hz | |
| | $SCKI = 128 f_S$ and $192 f_S$ | $0.569 \times f_S$ | | | Hz | |
| Stop band (quad) | | $0.569 \times f_S$ | | | Hz | |
| Passband ripple | $< 0.454 \times f_S$, $0.432 \times f_S$ | | | ± 0.0018 | dB | |
| Stop band attenuation | $> 0.546 \times f_S$, $0.569 \times f_S$ | -75 | | | dB | |

(1) In single-ended mode at V_{OUTx} pins, $f_{OUT} = 1\text{ kHz}$, using Audio Precision System II, Average mode with 20-kHz LPF and 400-Hz HPF.

(2) $f_S = 48\text{ kHz}$: $SCKI = 512 f_S$ (single), $f_S = 96\text{ kHz}$: $SCKI = 256 f_S$ (dual), $f_S = 192\text{ kHz}$: $SCKI = 128 f_S$ (quad).

ELECTRICAL CHARACTERISTICS: DAC (continued)

All specifications at $T_A = +25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $SCKI = 512 f_S$, 24-bit data, and Sampling mode = Auto, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | PCM1691 | | | UNIT |
|--|---------------------------------------|--------------------|-----------|--------------------|------|
| | | MIN | TYP | MAX | |
| DIGITAL FILTER PERFORMANCE WITH SLOW ROLL-OFF | | | | | |
| Passband | | | | $0.328 \times f_S$ | Hz |
| Stop band | | $0.673 \times f_S$ | | | Hz |
| Passband ripple | $< 0.328 \times f_S$ | | | ± 0.0013 | dB |
| Stop band attenuation | $> 0.673 \times f_S$ | -75 | | | dB |
| DIGITAL FILTER PERFORMANCE | | | | | |
| Group delay time (single, dual) | Except $SCKI = 128 f_S$ and $192 f_S$ | | $28/f_S$ | | sec |
| | $SCKI = 128 f_S$ and $192 f_S$ | | $19/f_S$ | | sec |
| Group delay time (quad) | | | $19/f_S$ | | sec |
| De-emphasis error | | | ± 0.1 | | dB |

ELECTRICAL CHARACTERISTICS: Power-Supply Requirements

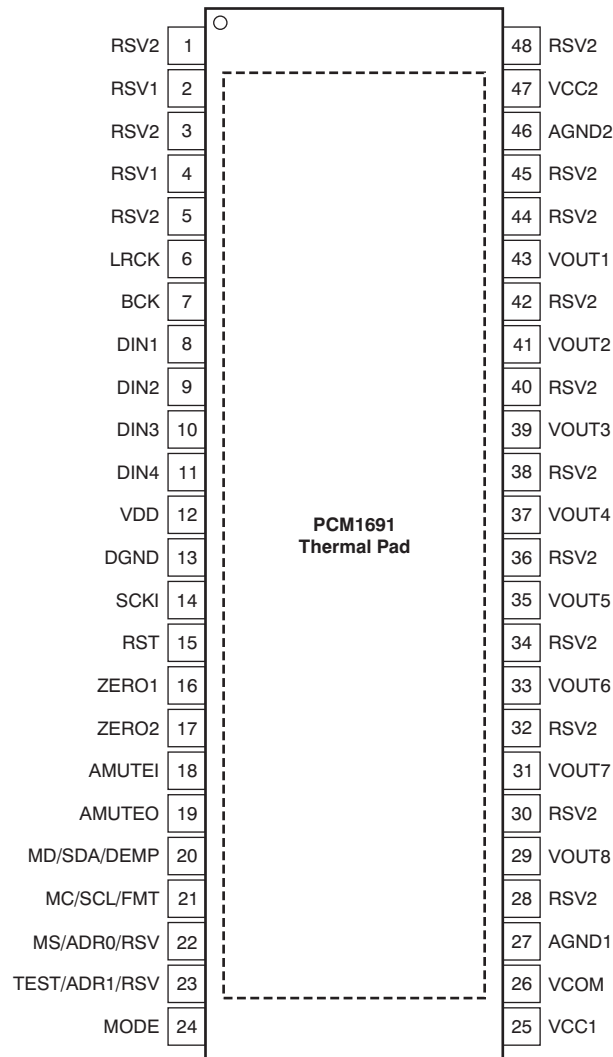
All specifications at $T_A = +25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $SCKI = 512 f_S$, 24-bit data, and Sampling mode = Auto, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | PCM1691 | | | UNIT |
|----------------------------------|---------------------------------|--------------------------------|------|-----|--------------------|
| | | MIN | TYP | MAX | |
| POWER-SUPPLY REQUIREMENTS | | | | | |
| Voltage range | $V_{CC1/2}$ | 4.5 | 5.0 | 5.5 | VDC |
| | VDD | 3.0 | 3.3 | 3.6 | VDC |
| Supply current | I_{CC} | $f_S = 48\text{ kHz}$ | 74 | 110 | mA |
| | | $f_S = 192\text{ kHz}$ | 74 | | mA |
| | | Full power-down ⁽¹⁾ | 170 | | μA |
| | I_{DD} | $f_S = 48\text{ kHz}$ | 57 | 90 | mA |
| | | $f_S = 192\text{ kHz}$ | 76 | | mA |
| | | Full power-down ⁽¹⁾ | 60 | | μA |
| Power dissipation | $f_S = 48\text{ kHz}$ | | 558 | 847 | mW |
| | $f_S = 192\text{ kHz}$ | | 621 | | mW |
| | Full power-down ⁽¹⁾ | | 1.05 | | mW |
| TEMPERATURE RANGE | | | | | |
| Operating temperature | PCM1691 consumer grade | -40 | | +85 | $^\circ\text{C}$ |
| Thermal resistance | θ_{JA} HTSSOP-48, High-K | | 23 | | $^\circ\text{C/W}$ |

(1) SCKI, BCK, and LRCK stopped.

PIN CONFIGURATION

DCA PACKAGE HTSSOP-48 (TOP VIEW)



TERMINAL FUNCTIONS

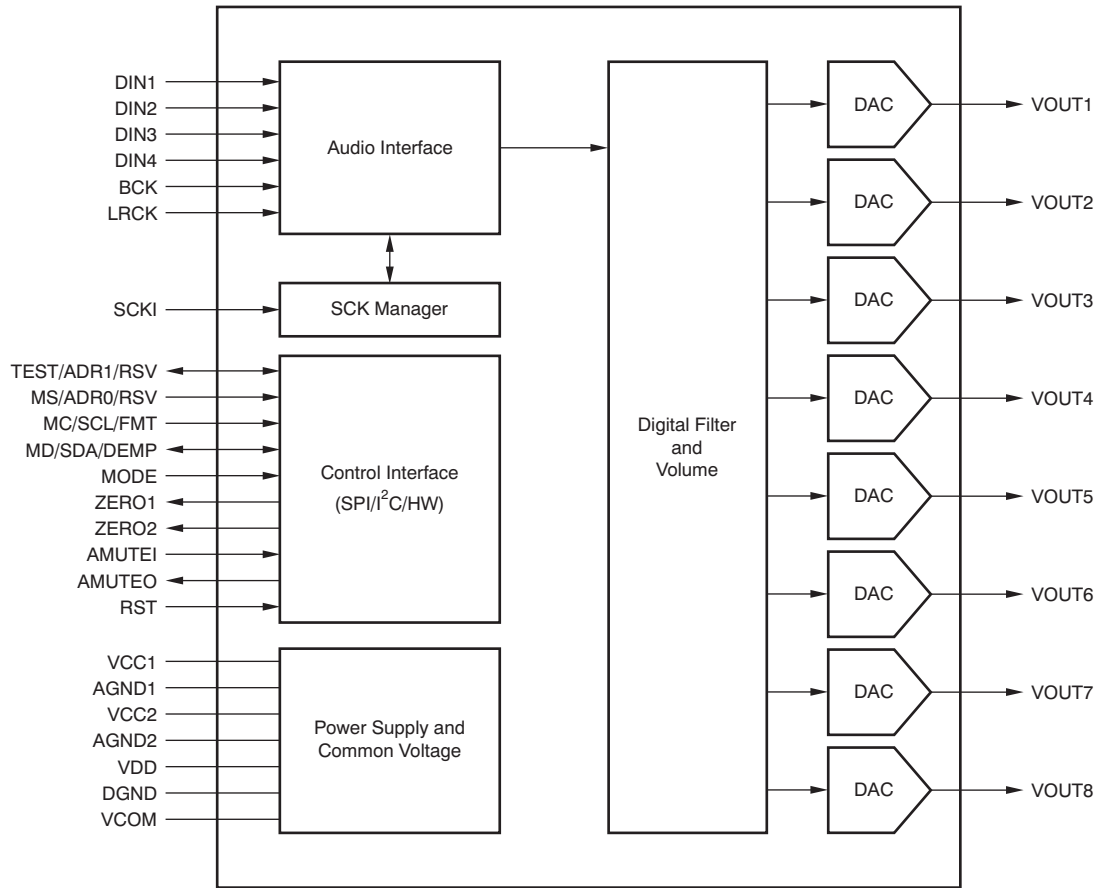
| TERMINAL | | I/O | PULL-DOWN | 5-V TOLERANT | DESCRIPTION |
|----------|-----|-----|-----------|--------------|------------------------------------|
| NAME | PIN | | | | |
| RSV2 | 1 | — | — | — | Reserved, tied to analog ground |
| RSV1 | 2 | — | — | — | Reserved, left open |
| RSV2 | 3 | — | — | — | Reserved, tied to analog ground |
| RSV1 | 4 | O | — | — | Reserved, left open |
| RSV2 | 5 | I | — | — | Reserved, tied to analog ground |
| LRCK | 6 | I/O | Yes | No | Audio data word clock input |
| BCK | 7 | I/O | Yes | No | Audio data bit clock input |
| DIN1 | 8 | I | No | No | Audio data input for DAC1 and DAC2 |
| DIN2 | 9 | I | No | No | Audio data input for DAC3 and DAC4 |
| DIN3 | 10 | I | No | No | Audio data input for DAC5 and DAC6 |
| DIN4 | 11 | I | No | No | Audio data input for DAC7 and DAC8 |

TERMINAL FUNCTIONS (continued)

| TERMINAL | | I/O | PULL-DOWN | 5-V TOLERANT | DESCRIPTION |
|---------------|-----|-----|-----------|--------------|---|
| NAME | PIN | | | | |
| VDD | 12 | — | — | — | Digital power supply, +3.3 V |
| DGND | 13 | — | — | — | Digital ground |
| SCKI | 14 | I | No | Yes | System clock input |
| RST | 15 | I | Yes | Yes | Reset and power-down control input with active low |
| ZERO1 | 16 | O | No | No | Zero detect flag output 1 |
| ZERO2 | 17 | O | No | No | Zero detect flag output 2 |
| AMUTEI | 18 | I | No | Yes | Analog mute control input with active low |
| AMUTE0 | 19 | O | No | Yes | Analog mute status output ⁽¹⁾ with active low |
| MD/SDA/DEMP | 20 | I/O | No | Yes | Input data for SPI, data for I ² C ⁽¹⁾ , de-emphasis control for hardware control mode |
| MC/SCL/FMT | 21 | I | No | Yes | Clock for SPI, clock for I ² C, format select for hardware control mode |
| MS/ADR0/RSV | 22 | I | Yes | Yes | Chip Select for SPI, address select 0 for I ² C, reserve (set low) for hardware control mode |
| TEST/ADR1/RSV | 23 | I/O | No | Yes | Test (factory use, left open) for SPI, address select 1 for I ² C, reserve (set low) for hardware control mode |
| MODE | 24 | I | No | No | Control port mode selection. Tied to VDD: SPI, left open: H/W mode, tied to DGND: I ² C |
| VCC1 | 25 | — | — | — | Analog power supply 1, +5 V |
| VCOM | 26 | — | — | — | Voltage common decoupling |
| AGND1 | 27 | — | — | — | Analog ground 1 |
| RSV2 | 28 | — | — | — | Reserved, tied to analog ground |
| VOUT8 | 29 | O | No | No | Analog output from DAC8 |
| RSV2 | 30 | — | — | — | Reserved, tied to analog ground |
| VOUT7 | 31 | O | No | No | Analog output from DAC7 |
| RSV2 | 32 | — | — | — | Reserved, tied to analog ground |
| VOUT6 | 33 | O | No | No | Analog output from DAC6 |
| RSV2 | 34 | — | — | — | Reserved, tied to analog ground |
| VOUT5 | 35 | O | No | No | Analog output from DAC5 |
| RSV2 | 36 | — | — | — | Reserved, tied to analog ground |
| VOUT4 | 37 | O | No | No | Analog output from DAC4 |
| RSV2 | 38 | — | — | — | Reserved, tied to analog ground |
| VOUT3 | 39 | O | No | No | Analog output from DAC3 |
| RSV2 | 40 | — | — | — | Reserved, tied to analog ground |
| VOUT2 | 41 | O | No | No | Analog output from DAC2 |
| RSV2 | 42 | — | — | — | Reserved, tied to analog ground |
| VOUT1 | 43 | O | No | No | Analog output from DAC1 |
| RSV2 | 44 | — | — | — | Reserved, tied to analog ground |
| RSV2 | 45 | — | — | — | Reserved, tied to analog ground |
| AGND2 | 46 | — | — | — | Analog ground 2 |
| VCC2 | 47 | — | — | — | Analog power supply 2, +5 V |
| RSV2 | 48 | — | — | — | Reserved, tied to analog ground |

(1) Open-drain configuration in out mode.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS: Digital Filter

All specifications at $T_A = +25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCKI} = 512 f_S$, 24-bit data, and Sampling mode = Auto, unless otherwise noted.

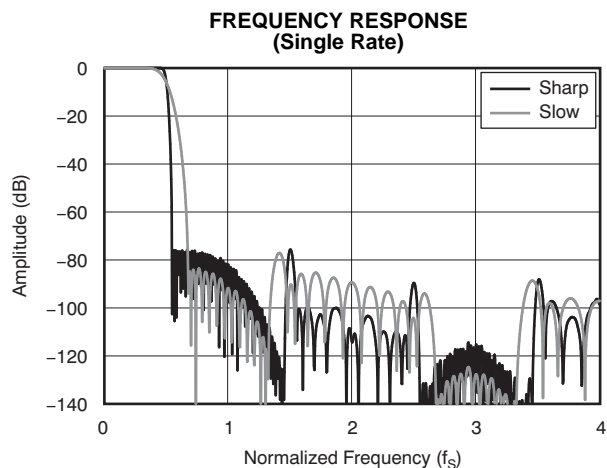


Figure 1.

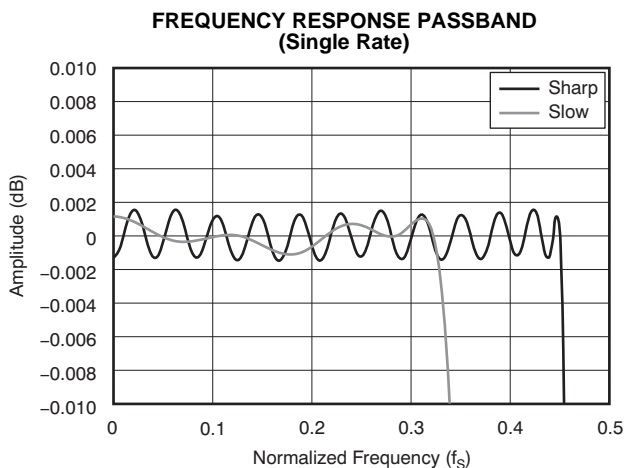


Figure 2.

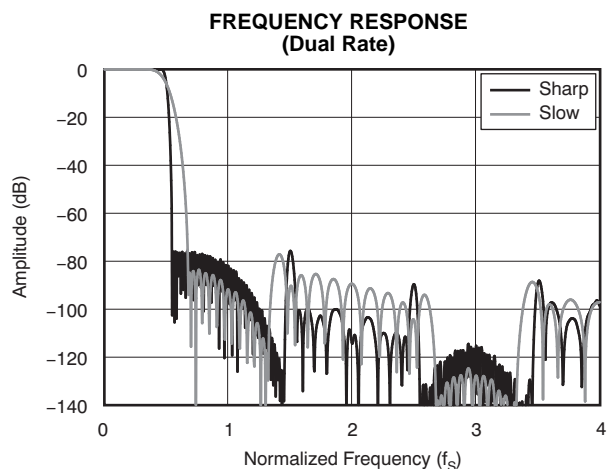


Figure 3.

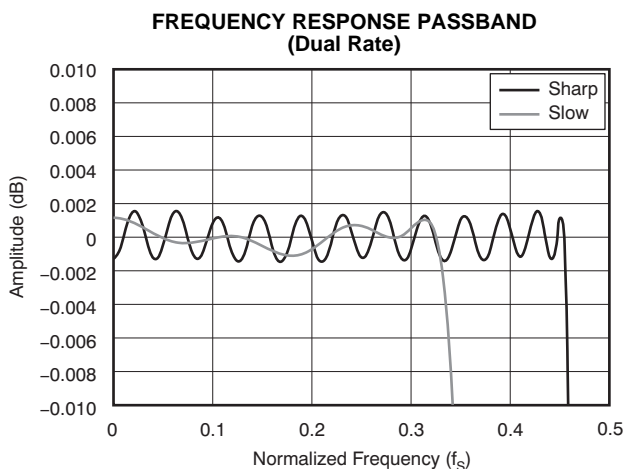


Figure 4.

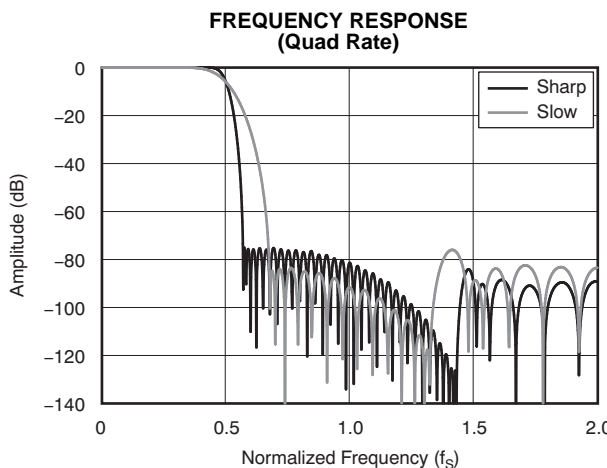


Figure 5.

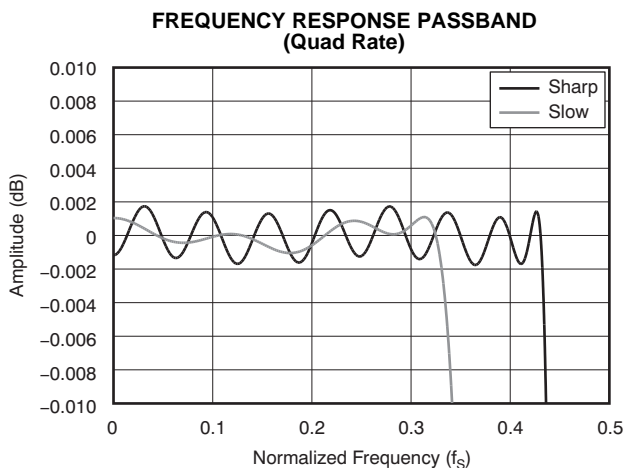


Figure 6.

TYPICAL CHARACTERISTICS: Digital De-Emphasis Filter

All specifications at $T_A = +25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCKI} = 512 f_S$, 24-bit data, and Sampling mode = Auto, unless otherwise noted.

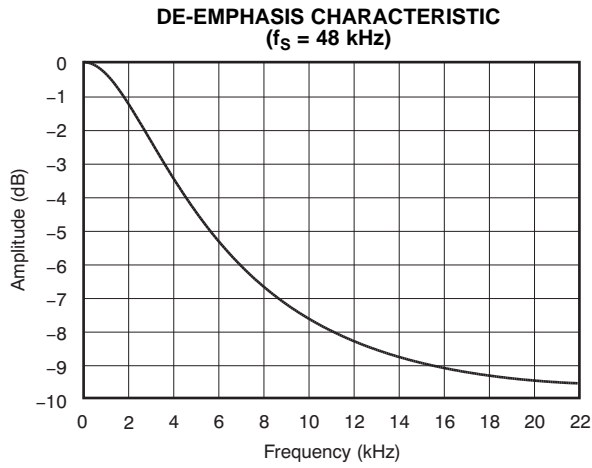


Figure 7.

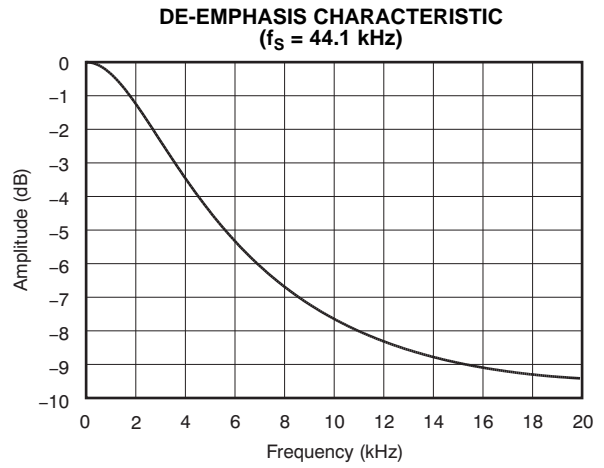


Figure 8.

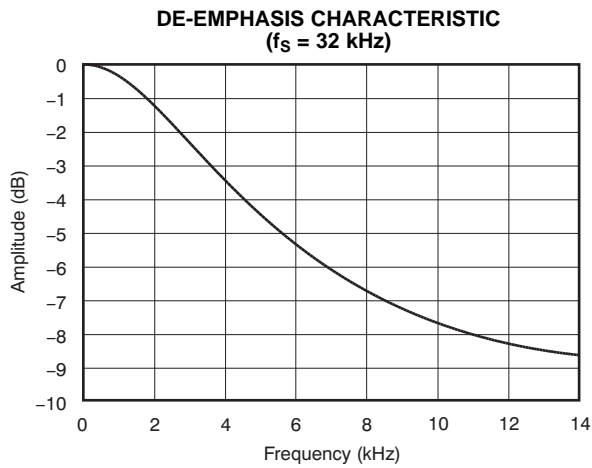


Figure 9.

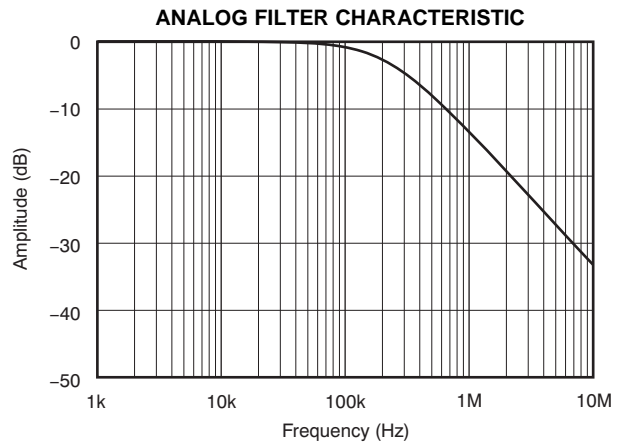


Figure 10.

TYPICAL CHARACTERISTICS: Dynamic Performance

All specifications at $T_A = +25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $SCKI = 512\text{ f}_S$, 24-bit data, and Sampling mode = Auto, unless otherwise noted.

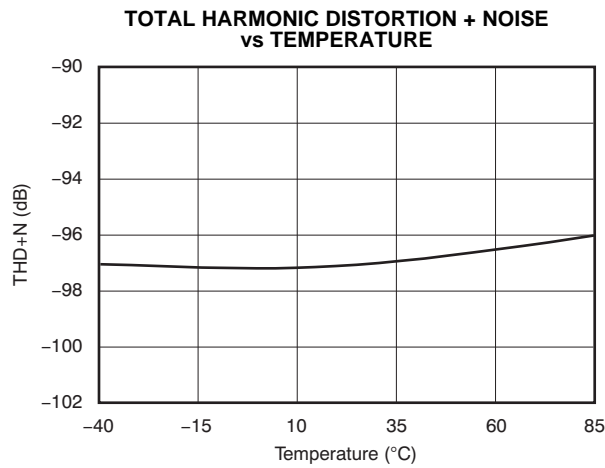


Figure 11.

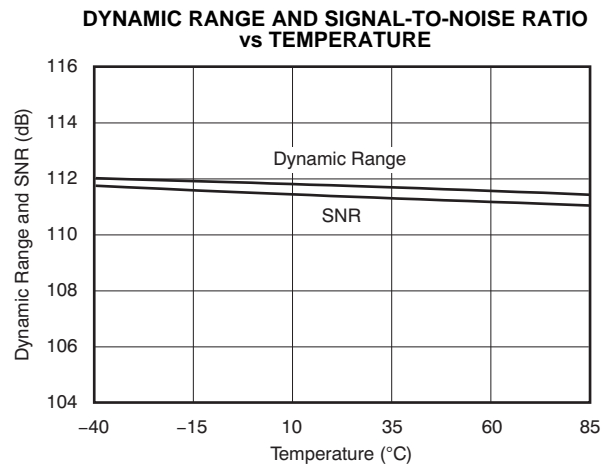


Figure 12.

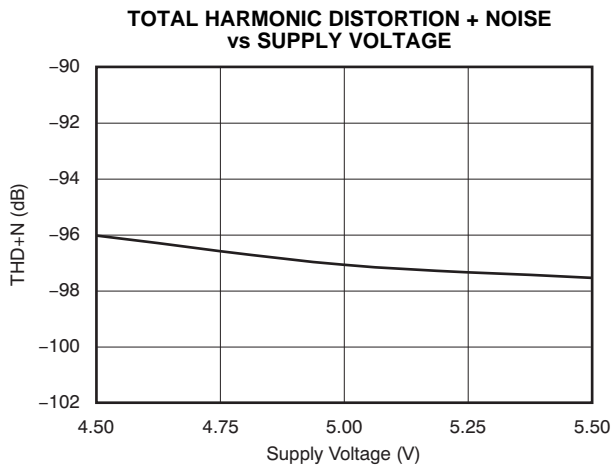


Figure 13.

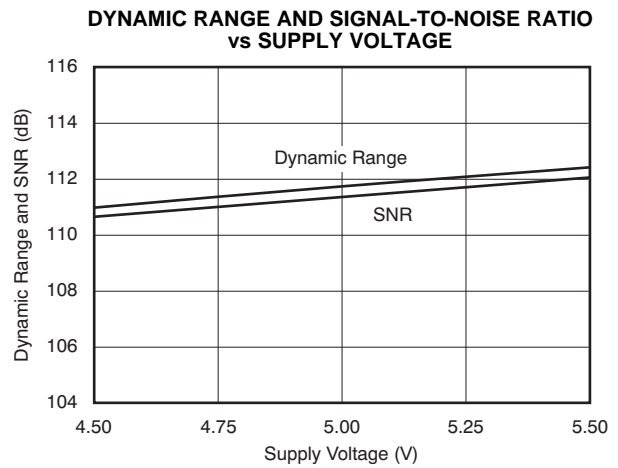
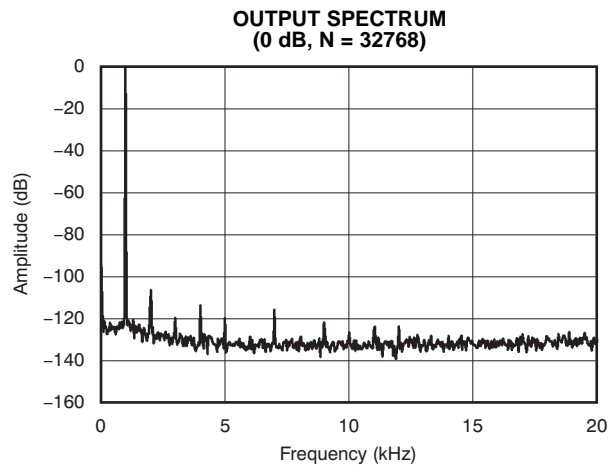
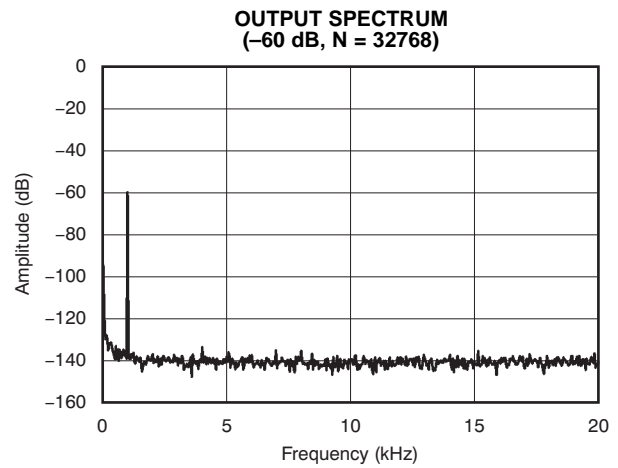
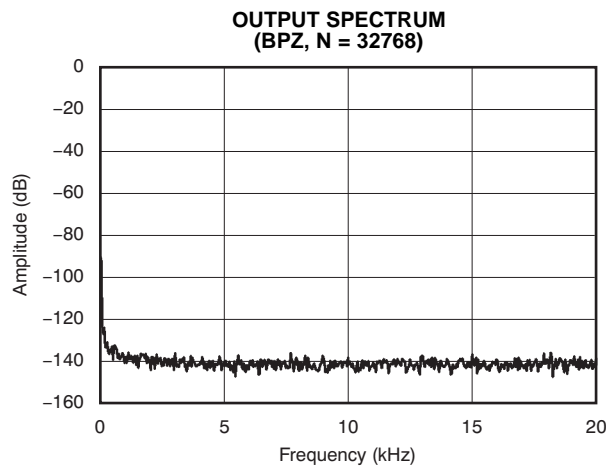


Figure 14.

TYPICAL CHARACTERISTICS: Output Spectrum

All specifications at $T_A = +25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCKI} = 512 f_S$, 24-bit data, and Sampling mode = Auto, unless otherwise noted.

**Figure 15.****Figure 16.****Figure 17.**

PRODUCT OVERVIEW

The PCM1691 is a high-performance, multi-channel DAC targeted for consumer audio applications such as Blu-ray Disc players and DVD players, as well as home multi-channel audio applications (such as home theater systems and A/V receivers). The PCM1691 consists of an eight-channel DAC. The DAC output type is fixed with a single-ended configuration. The PCM1691 supports 16-/20-/24-/32-bit linear PCM input data in I²S and left-justified audio formats, and 24-bit linear PCM input data in right-justified, DSP, and TDM formats with various sampling frequencies from 8 kHz to 192 kHz. The TDM format is useful for saving the interface bus line number for multi-channel audio data communication between the DAC and the digital audio processor. The PCM1691 offers three modes for device control: two-wire I²C software, three-wire SPI software, and hardware.

ANALOG OUTPUTS

The PCM1691 includes an eight-channel DAC, with single-ended voltage outputs pins. The full-scale output voltage is $(0.8 \times V_{CC1}) V_{PP}$ in single-ended output mode. These single-ended outputs are each capable of driving $0.8 \times V_{CC1}$ ($4 V_{PP}$) typical into a 5-k Ω ac-coupled load with $V_{CC1} = +5$ V. The internal output amplifiers for VOUT1 through VOUT8 are biased to the dc common voltage, equal to $(0.5 \times V_{CC1})$.

The output amplifiers include an RC continuous-time filter that helps to reduce the out-of-band noise energy present at the DAC outputs as a result of the noise shaping characteristics of the PCM1691 delta-sigma ($\Delta\Sigma$) DACs. The frequency response of this filter is shown in the *Analog Filter Characteristic* (Figure 10) of the [Typical Characteristics](#). By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the [Application Information](#) section.

Table 1. Pin Assignments in Single-Ended Output Mode

| DIGITAL INPUT | CHANNEL | SINGLE-ENDED OUTPUT |
|---------------|----------|---------------------|
| DIN1 | 1 (DAC1) | VOUT1 |
| | 2 (DAC2) | VOUT2 |
| DIN2 | 3 (DAC3) | VOUT3 |
| | 4 (DAC4) | VOUT4 |
| DIN3 | 5 (DAC5) | VOUT5 |
| | 6 (DAC6) | VOUT6 |
| DIN4 | 7 (DAC7) | VOUT7 |
| | 8 (DAC8) | VOUT8 |

VOLTAGE REFERENCE VCOM

The PCM1691 includes a pin for the common-mode voltage output, VCOM. This pin should be connected to the analog ground via a decoupling capacitor. This pin can also be used to bias external high-impedance circuits, if they are required.

SYSTEM CLOCK INPUT

The PCM1691 requires an external system clock input applied at the SCKI input for DAC operation. The system clock operates at an integer multiple of the sampling frequency, or f_s . The multiples supported in DAC operation include $128 f_s$, $192 f_s$, $256 f_s$, $384 f_s$, $512 f_s$, $768 f_s$, and $1152 f_s$. Details for these system clock multiples are shown in [Table 2](#). [Figure 18](#) and [Table 3](#) show the SCKI timing requirements.

Table 2. System Clock Frequencies for Common Audio Sampling Rates

| DEFAULT SAMPLING MODE | SAMPLING FREQUENCY, f_s (kHz) | SYSTEM CLOCK FREQUENCY (MHz) | | | | | | |
|-----------------------|---------------------------------|------------------------------|-----------|-----------|-----------|-----------|-----------|------------|
| | | $128 f_s$ | $192 f_s$ | $256 f_s$ | $384 f_s$ | $512 f_s$ | $768 f_s$ | $1152 f_s$ |
| Single rate | 8 | N/A | N/A | 2.0480 | 3.0720 | 4.0960 | 6.1440 | 9.2160 |
| | 16 | 2.0480 | 3.0720 | 4.0960 | 6.1440 | 8.1920 | 12.2880 | 18.4320 |
| | 32 | 4.0960 | 6.1440 | 8.1920 | 12.2880 | 16.3840 | 24.5760 | 36.8640 |
| | 44.1 | 5.6448 | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A |
| | 48 | 6.1440 | 9.2160 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A |
| Dual rate | 88.2 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | N/A | N/A | N/A |
| | 96 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | N/A | N/A | N/A |
| Quad rate | 176.4 | 22.5792 | 33.8688 | N/A | N/A | N/A | N/A | N/A |
| | 192 | 24.5760 | 36.8640 | N/A | N/A | N/A | N/A | N/A |

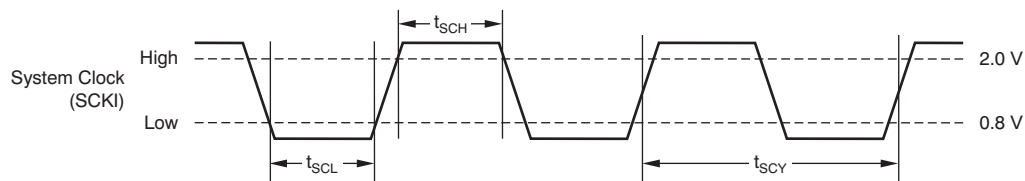


Figure 18. System Clock Timing Diagram

Table 3. Timing Requirements for [Figure 18](#)

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-----------|-------------------------|-----|-----|------|
| t_{SCY} | System clock cycle time | 27 | | ns |
| t_{SCH} | System clock width high | 10 | | ns |
| t_{SCL} | System clock width low | 10 | | ns |
| — | System clock duty cycle | 40 | 60 | % |

SAMPLING MODE

The PCM1691 supports three sampling modes (single rate, dual rate, and quad rate) in DAC operation. In single rate mode, the DAC operates at an oversampling frequency of x128 (except when $SCK1 = 128 f_s$ and $192 f_s$); this mode is supported for sampling frequencies less than 50 kHz. In dual rate mode, the DAC operates at an oversampling frequency of x64; this mode is supported for sampling frequencies less than 100 kHz. In quad rate mode, the DAC operates at an oversampling frequency of x32. The sampling mode is automatically selected according to the ratio of system clock frequency and sampling frequency by default (that is, single rate for $512 f_s$, $768 f_s$, and $1152 f_s$; dual rate for $256 f_s$ and $384 f_s$; and quad rate for $128 f_s$ and $192 f_s$), but manual selection is also possible for specified combinations through the serial mode control register.

Table 4 and Figure 19 show the relationship among the oversampling rate (OSR) of the digital filter and $\Delta\Sigma$ modulator, the noise-free shaped bandwidth, and each sampling mode setting.

Table 4. Digital Filter OSR, Modulator OSR, and Noise-Free Shaped Bandwidth for Each Sampling Mode

| SAMPLING MODE REGISTER SETTING | SYSTEM CLOCK FREQUENCY (xf_s) | NOISE-FREE SHAPED BANDWIDTH ⁽¹⁾ (kHz) | | | DIGITAL FILTER OSR | MODULATOR OSR |
|--------------------------------|-----------------------------------|--|----------------|-----------------|--------------------|---------------|
| | | $f_s = 48$ kHz | $f_s = 96$ kHz | $f_s = 192$ kHz | | |
| Auto | 512, 768, 1152 | 40 | N/A | N/A | x8 | x128 |
| | 256, 384 | 20 | 40 | N/A | x8 | x64 |
| | 128, 192 ⁽²⁾ | 10 | 20 | 40 | x4 | x32 |
| Single | 512, 768, 1152 | 40 | N/A | N/A | x8 | x128 |
| | 256, 384 | 40 | N/A | N/A | x8 | x128 |
| | 128, 192 ⁽²⁾ | 20 | N/A | N/A | x4 | x64 |
| Dual | 256, 384 | 20 | 40 | N/A | x8 | x64 |
| | 128, 192 ⁽²⁾ | 20 | 40 | N/A | x4 | x64 |
| Quad | 128, 192 ⁽²⁾ | 10 | 20 | 40 | x4 | x32 |

- (1) Bandwidth in which noise is shaped out.
- (2) Quad mode filter characteristic is applied.

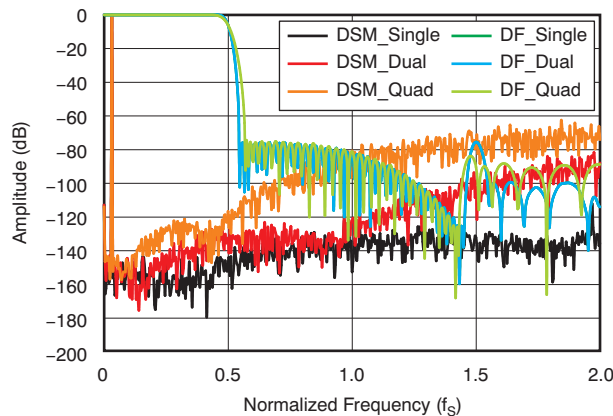


Figure 19. $\Delta\Sigma$ Modulator and Digital Filter Characteristic

RESET OPERATION

The PCM1691 has both an internal power-on reset circuit and an external reset circuit. The sequences for both reset circuits are shown in [Figure 20](#) and [Figure 21](#). [Figure 20](#) illustrates the timing at the internal power-on reset. Initialization is triggered automatically at the point where VDD exceeds 2.2 V typical, and the internal reset is released after 3846 SCKI clock cycles from power-on, if RST is held high and SCKI is provided. VOUTx from the DAC is forced to the VCOM level initially (that is, $0.5 \times VCC1$) and settles at a specified level according to the rising VCC. If synchronization among SCKI, BCK, and LRCK is maintained, VOUTx provides an output that corresponds to DINx after 3846 SCKI clocks from power-on. If the synchronization is not held, the internal reset is not released, and both operating modes are maintained at reset and power-down states. After synchronization forms again, the DAC returns to normal operation with the previous sequences.

[Figure 21](#) illustrates a timing diagram at the external reset. RST accepts an externally-forced reset with RST low, and provides a device reset and power-down state that achieves the lowest power dissipation state available in the PCM1691. If RST goes from high to low under synchronization among SCKI, BCK, and LRCK, the internal reset is asserted, all registers and memory are reset, and finally, the PCM1691 enters into all power-down states. At the same time, VOUTx is immediately forced into the AGND1 level. To begin normal operation again, toggle RST high; the same power-up sequence is performed as the power-on reset shown in [Figure 20](#).

The PCM1691 does not require particular power-on sequences for VCC and VDD; it allows VDD on and then VCC on, or VCC on and then VDD on. From the viewpoint of the [Absolute Maximum Ratings](#), however, simultaneous power-on is recommended for avoiding unexpected responses on VOUTx. [Figure 20](#) illustrates the response for VCC on with VDD on.

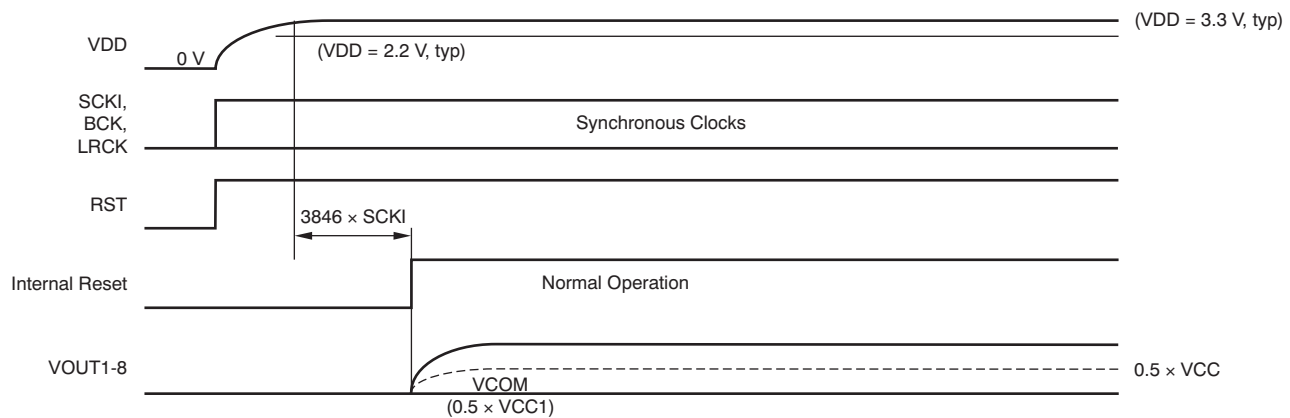


Figure 20. Power-On-Reset Timing Requirements

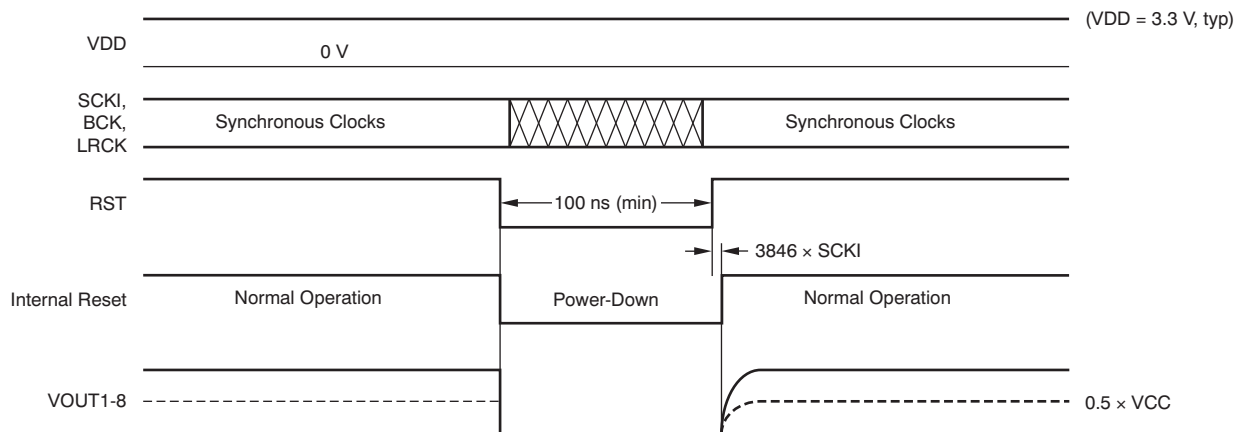


Figure 21. External Reset Timing Requirements

AUDIO SERIAL PORT OPERATION

The PCM1691 audio serial port consists of six signals: BCK, LRCK, DIN1, DIN2, DIN3, and DIN4. BCK is a bit clock input. LRCK is a left/right word clock or frame synchronization clock input. DIN1 through DIN4 are the audio data inputs for VOUT1 through VOUT8.

AUDIO DATA INTERFACE FORMATS AND TIMING

The PCM1691 supports 10 audio data interface formats: 16-/20-/24-/32-bit I²S, 16-/20-/24-/32-bit left-justified, 24-bit right-justified, 16-bit right-justified, 24-bit left-justified mode DSP, 24-bit I²S mode DSP, 24-bit left-justified mode TDM, 24-bit I²S mode TDM, 24-bit left-justified mode high-speed TDM, and 24-bit I²S mode high-speed TDM. In the case of I²S, left-justified, and right-justified data formats, 64 BCKs, 48 BCKs, and 32 BCKs per LRCK period are supported; however, 48 BCKs are limited to 192/384/768 f_S SCKI, and 32 BCKs are limited to 16-bit right-justified only. In the case of TDM data format in single rate, BCK, LRCK, and DIN1 are used. In the case of TDM data format in dual rate, BCK, LRCK, and DIN1/2 are used. In the case of high-speed TDM format in quad rate, BCK, LRCK, and DIN1/2 are used. TDM format and high-speed TDM format are supported only at SCKI = 512 f_S, 256 f_S, 128 f_S, and f_{BCK} ≤ f_{SCKI}. The audio data formats are selected by MC/SCL/FMT in hardware control mode and by the FMTDA[3:0] bits in control register 65 (41h) in software control mode. All data must be in binary two's complement and MSB first.

Table 5 summarizes the applicable formats and describes the relationships among them and the respective restrictions with mode control. Figure 22 through Figure 28 show the 10 audio interface data formats.

Table 5. Audio Data Interface Formats and Sampling Rate, Bit Clock, and System Clock Restrictions

| CONTROL MODE | FORMAT | DATA BITS | MAX LRCK FREQUENCY (f _S) | SCKI RATE (xf _S) | BCK RATE (xf _S) | APPLICABLE PINS | |
|------------------|--|----------------------------|--------------------------------------|------------------------------|------------------------------------|-----------------|--------|
| Software control | I ² S/Left-Justified | 16/20/24/32 ⁽¹⁾ | 192 kHz | 128 to 1152 ⁽²⁾ | 64, 48 | DIN1/2/3/4 | |
| | Right-Justified | 24, 16 | 192 kHz | 128 to 1152 ⁽²⁾ | 64, 48, 32 (16 bit) ⁽³⁾ | DIN1/2/3/4 | |
| | I ² S/Left-Justified DSP | 24 | 192 kHz | 128 to 768 | 64 | DIN1/2/3/4 | |
| | I ² S/ Left-Justified TDM | | 24 | 48 kHz | 256, 512 | 256 | DIN1 |
| | | | 24 | 96 kHz | 128, 256 | 128 | DIN1/2 |
| | High-Speed I ² S/Left-Justified TDM | 24 | 96 kHz | 256 | 256 | DIN1 | |
| Hardware control | I ² S | 16/20/24/32 ⁽¹⁾ | 192 kHz | 128 to 1152 ⁽²⁾ | 64, 48 | DIN1/2/3/4 | |
| | | 24 | 48 kHz | 512 | 256 | DIN1 | |
| | I ² S TDM | 24 | 96 kHz | 256 | 128 | DIN1/2 | |

- (1) 32-bit data length is acceptable only for BCK = 64 f_S and when using the I²S or Left-Justified format.
 (2) 1152 f_S is acceptable only for f_S = 32 kHz, BCK = 64 f_S, and when using the I²S, Left-Justified, or 24-bit Right-Justified formats.
 (3) BCK = 32 f_S is supported only for 16-bit data length.

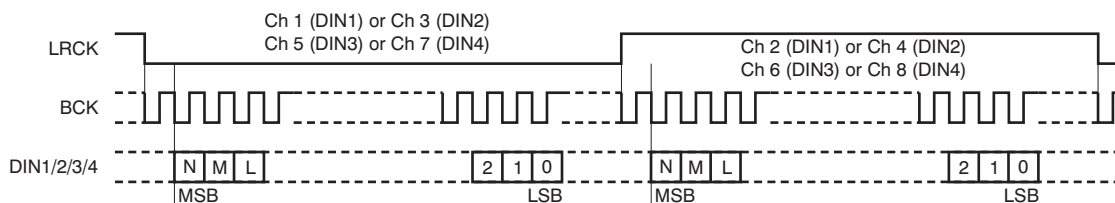


Figure 22. Audio Data Format: 16-/20-/24-/32-Bit I²S
 (N = 15/19/23/31, M = 14/18/22/30, and L = 13/17/21/29)

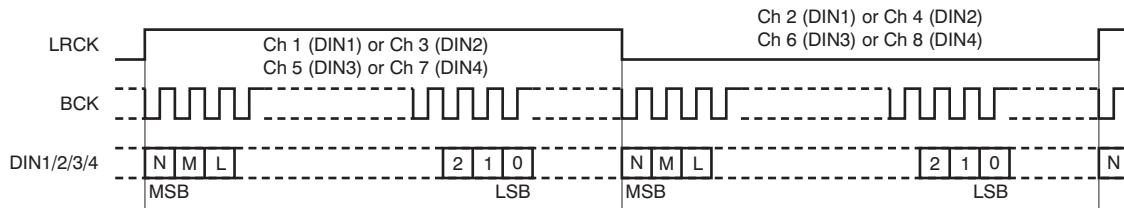


Figure 23. Audio Data Format: 16-/20-/24-/32-Bit Left-Justified
 (N = 15/19/23/31, M = 14/18/22/30, and L = 13/17/21/29)

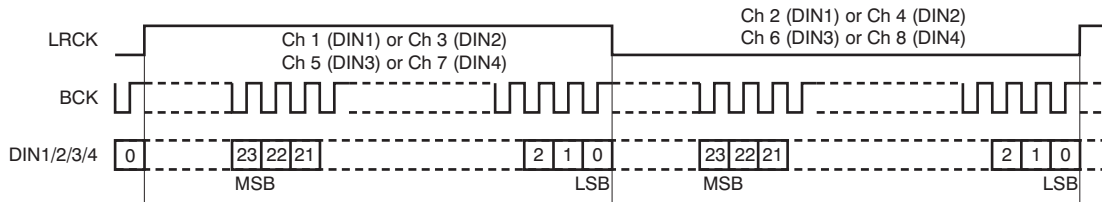


Figure 24. Audio Data Format: 24-Bit Right-Justified

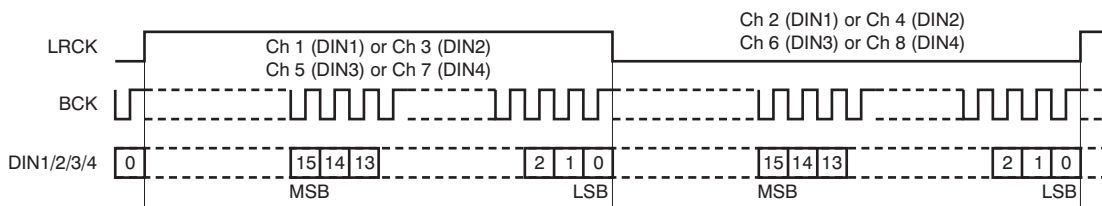


Figure 25. Audio Data Format: 16-Bit Right-Justified

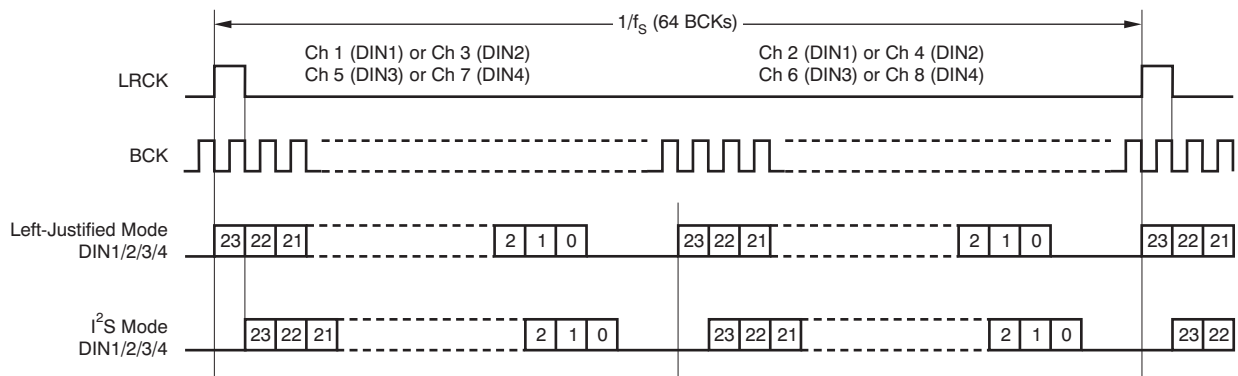


Figure 26. Audio Data Format: 24-Bit DSP Format

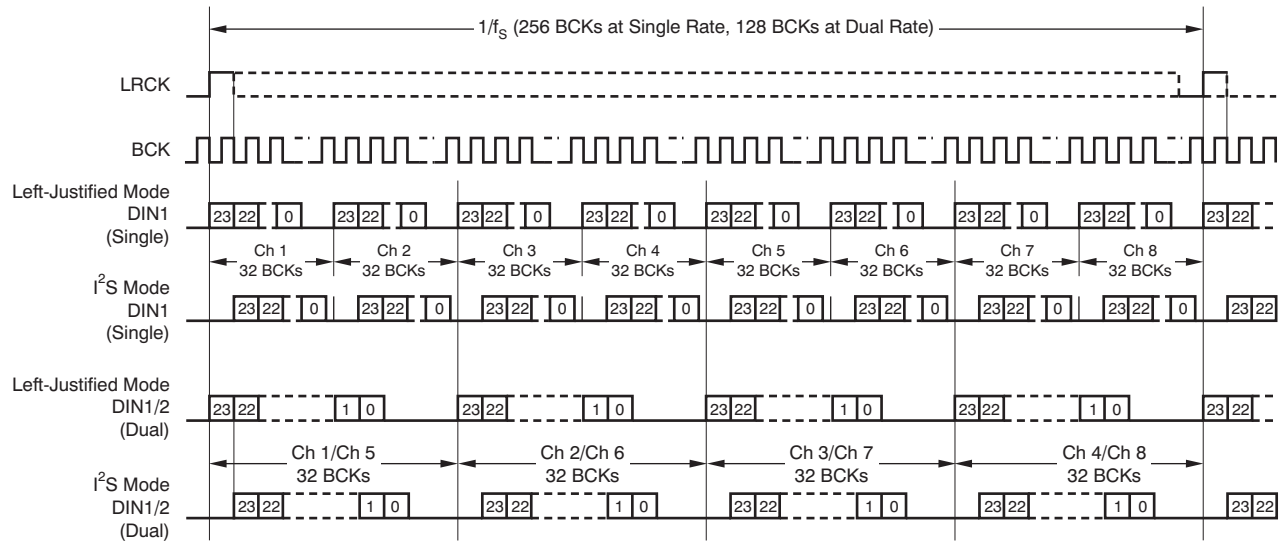


Figure 27. Audio Data Format: 24-Bit TDM Format (SCKI = 128 f_s, 256 f_s, and 512 f_s Only)

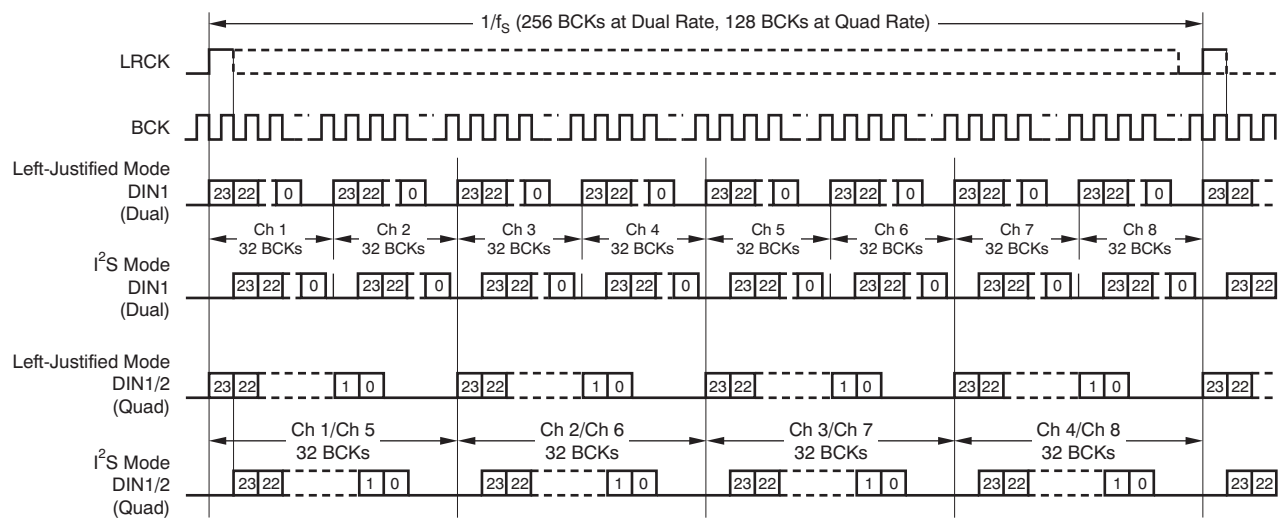


Figure 28. Audio Data Format: 24-Bit High-Speed TDM Format (SCKI = 128 f_s and 256 f_s Only)

AUDIO INTERFACE TIMING

Figure 29 and Table 6 describe the detailed audio interface timing specifications.

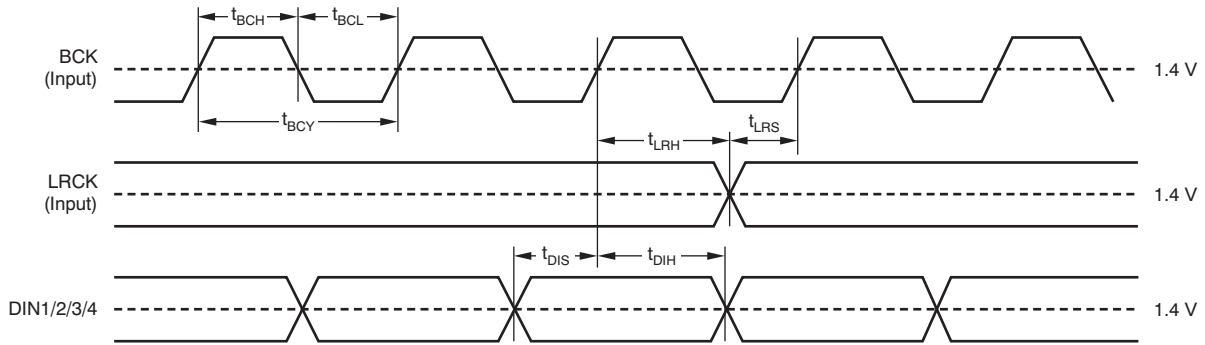


Figure 29. Audio Interface Timing Diagram for Left-Justified, Right-Justified, I²S, and DSP Data Formats

Table 6. Timing Requirements for Figure 29

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| t _{BCY} | BCK cycle time | 75 | | | ns |
| t _{BCH} | BCK pulse width high | 35 | | | ns |
| t _{BCL} | BCK pulse width low | 35 | | | ns |
| t _{LRS} | LRCK setup time to BCK rising edge | 10 | | | ns |
| t _{LRH} | LRCK hold time to BCK rising edge | 10 | | | ns |
| t _{DIS} | DIN1/2/3/4 setup time to BCK rising edge | 10 | | | ns |
| t _{DIH} | DIN1/2/3/4 hold time to BCK rising edge | 10 | | | ns |

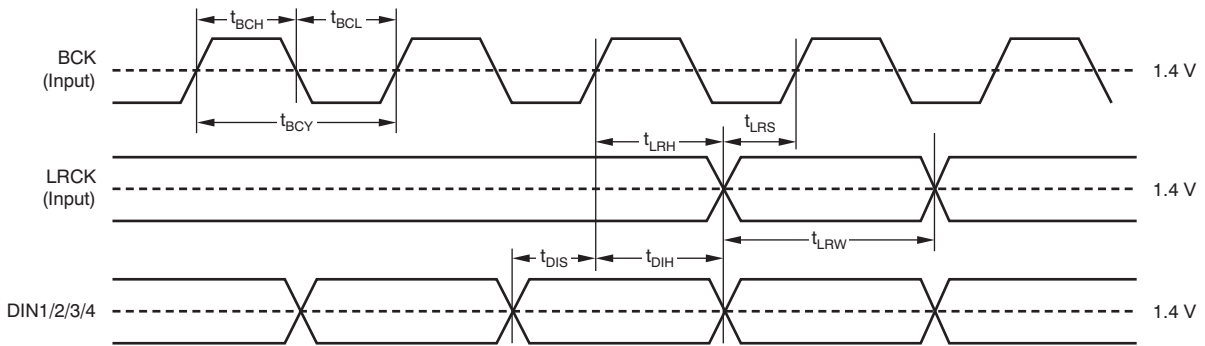


Figure 30. Audio Interface Timing Requirements for DSP and TDM Data Formats

Table 7. Timing Requirements for Figure 29

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------------|--|------------------|-----|-------------------------------------|------|
| t _{BCY} | BCK cycle time | 40 | | | ns |
| t _{BCH} | BCK pulse width high | 15 | | | ns |
| t _{BCL} | BCK pulse width low | 15 | | | ns |
| t _{LRW} | LRCK pulse width high (DSP format) | t _{BCY} | | t _{BCY} | sec |
| | LRCK pulse width high (TDM format) | t _{BCY} | | 1/f _S – t _{BCY} | sec |
| t _{LRS} | LRCK setup time to BCK rising edge | 10 | | | ns |
| t _{LRH} | LRCK hold time to BCK rising edge | 10 | | | ns |
| t _{DIS} | DIN1/2/3/4 setup time to BCK rising edge | 10 | | | ns |
| t _{DIH} | DIN1/2/3/4 hold time to BCK rising edge | 10 | | | ns |

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

The PCM1691 operates under the system clock (SCKI) and the audio sampling rate (LRCK). Therefore, SCKI and LRCK must have a specific relationship. The PCM1691 does not need a specific phase relationship between the audio interface clocks (LRCK, BCK) and the system clock (SCKI), but does require a specific frequency relationship (ratiometric) between LRCK, BCK, and SCKI.

If the relationship between SCKI and LRCK changes more than ± 2 BCK clocks because of jitter, sampling frequency change, etc., the DAC internal operation stops within $1/f_s$, and the analog output is forced into VCOM ($0.5 V_{CC1}$) until re-synchronization among SCKI, LRCK, and BCK completes, and then either $38/f_s$ (single, dual rate) or $29/f_s$ (quad rate) passes. In the event the change is less than ± 2 BCKs, re-synchronization does not occur, and this analog output control and discontinuity does not occur.

Figure 31 shows the DAC analog output during loss of synchronization. During undefined data periods, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined (or zero) data to normal data creates a discontinuity of data on the analog outputs, which may then generate some noise in the audio signal.

The DAC outputs (V_{OUTx}) hold the previous state if the system clock halts, but the asynchronous and re-synchronization processes will occur after the system clock resumes.

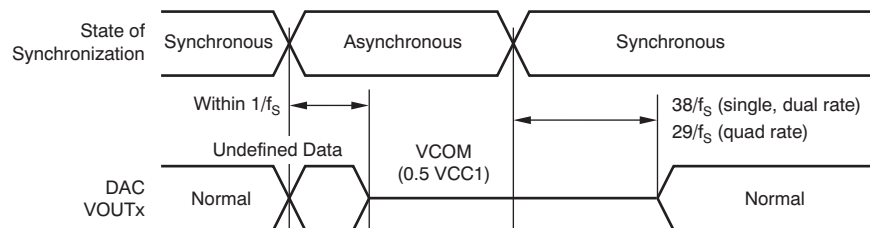


Figure 31. DAC Outputs During Loss of Synchronization

ZERO FLAG

The PCM1691 has two ZERO flag pins (ZERO1 and ZERO2) that can be assigned to the combinations shown in Table 8. Zero flag combinations are selected through the AZRO[1:0] bits in control register 70 (46h). If the input data of all the assigned channels remain at '0' for 1024 sampling periods (LRCK clock periods), the ZERO1/2 bits are set to a high level, logic '1' state. Furthermore, if the input data of any of the assigned channels read '1', the ZERO1/2 are set to a low level, logic '0' state, immediately. Zero data detection is supported for 16-/20-/24-bit data width, but is not supported for 32-bit data width.

The active polarity of the zero flag output can be inverted through the ZREV bit in control register 70 (46h). The reset default is active high for zero detection.

In parallel hardware control mode, ZERO1 and ZERO2 are fixed with combination A, shown in Table 8.

Table 8. Zero Flag Outputs Combination

| ZERO FLAG COMBINATION | ZERO1 | ZERO2 |
|-----------------------|--------------------|---------------------|
| A | DIN1, left channel | DIN1, right channel |
| B | DIN1–4 | DIN1–4 |
| C | DIN4 | DIN1–3 |
| D | DIN1 | DIN2–4 |

AMUTE CONTROL

The PCM1691 has an AMUTE control input, status output pins, and functionality. AMUTEI is the input control pin of the internal analog mute circuit. An AMUTEI low input causes the DAC output to cut off from the digital input and forces it to the center level ($0.5 \times VCC1$). AMUTEO is the status output pin of the internal analog mute circuit. AMUTEO low indicates the analog mute control circuit is active because of a programmed condition (such as an SCKI halt, asynchronous detect, zero detect, or by the DAC disable command) that forces the DAC outputs to a center level. Because AMUTEI is not terminated internally and AMUTEO is an open-drain output, pull-ups by the appropriate resistors are required for proper operation.

Additionally, because the AMUTEI pin control and power-down control in register (OPEDA[3:0] when high, PSM DA when low) do not function together, AMUTEI takes priority over power-down control. Therefore, power-down control is ignored during AMUTEI low, and AMUTEI low forces the DAC output to a center level ($0.5 \times VCC1$) even if power-down control is asserted.

MODE CONTROL

The PCM1691 includes three mode control interfaces with two oversampling configurations, depending on the input state of the MODE pin, as shown in [Table 9](#). The pull-up and pull-down resistors must each be less than 10 k Ω .

Table 9. Interface Mode Control Selection

| MODE | MODE CONTROL INTERFACE |
|-------------------|---|
| Tied to DGND, low | Two-wire (I ² C) serial control, selectable oversampling configuration |
| Left open | Two-wire parallel control, auto mode oversampling configuration |
| Tied to VDD, high | Three-wire (SPI) serial control, selectable oversampling configuration |

The input state of the MODE pin is sampled at the moment of power-on, or during a low-to-high transition of the RST pin, with the system clock input. Therefore, input changes after reset are ignored until the next power-on or reset. From the mode control selection described in [Table 9](#), the functions of four pins are changed, as shown in [Table 10](#).

Table 10. Pin Functions for Interface Mode

| PIN | PIN ASSIGNMENTS | | |
|-----|---------------------|--------------------|------------------|
| | SPI | I ² C | H/W |
| 20 | MD (input) | SDA (input/output) | DEMP (input) |
| 21 | MC (input) | SCL (input) | FMT (input) |
| 22 | MS (input) | ADR0 (input) | RSV (input, low) |
| 23 | Test (output, open) | ADR1 (input) | RSV (input, low) |

In serial mode control, the actual mode control is performed by register writes (and reads) through the SPI- or I²C-compatible serial control port. In parallel mode control, two specific functions are controlled directly through the high/low control of two specific pins, as described in the following section.

PARALLEL HARDWARE CONTROL

The functions shown in [Table 11](#) and [Table 12](#) are controlled by two pins, DEMP and FMT, in parallel hardware control mode. The DEMP pin controls the 44.1-kHz digital de-emphasis function of all eight channels. The FMT pin controls the audio interface format for all eight channels.

Table 11. DEMP Functionality

| DEMP | DESCRIPTION |
|------|-------------------------|
| Low | De-emphasis off |
| High | 44.1-kHz de-emphasis on |

Table 12. FMT Functionality

| FMT | DESCRIPTION |
|------|--|
| Low | 16-/20-/24-/32-bit I ² S format |
| High | 24-bit I ² S mode TDM format |

THREE-WIRE (SPI) SERIAL CONTROL

The PCM1691 includes an SPI-compatible serial port that operates asynchronously with the audio serial interface. The control interface consists of MD/SDA/DEMP, MC/SCL/FMT, and MS/ADR0/RSV. MD is the serial data input used to program the mode control registers. MC is the serial bit clock that shifts the data into the control port. MS is the select input used to enable the mode control port.

CONTROL DATA WORD FORMAT

All single write operations via the serial control port use 16-bit data words. Figure 32 shows the control data word format. The first bit (fixed at '0') is for write operation. After the first bit are seven other bits, labeled ADR[6:0], that set the register address for the write operation. The eight least significant bits (LSBs), D[7:0] on MD, contain the data to be written to the register address specified by ADR[6:0].

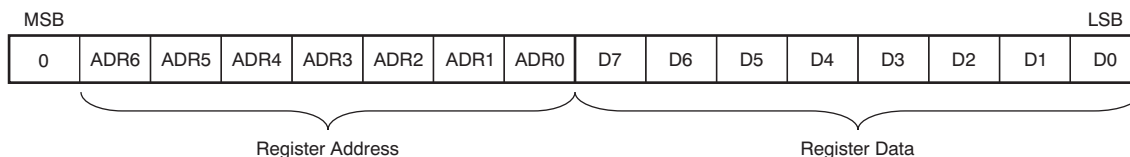
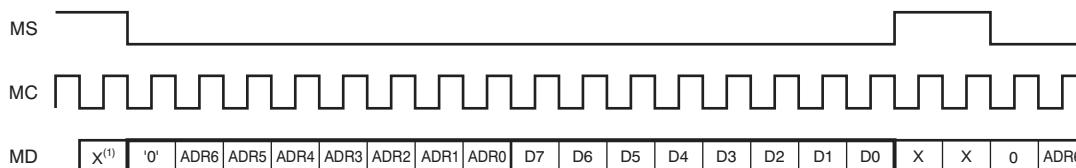


Figure 32. Control Data Word Format for MD

REGISTER WRITE OPERATION

Figure 33 shows the functional timing diagram for single write operations on the serial control port. MS is held at a high state until a register is to be written to. To start the register write cycle, MS is set to a low state. 16 clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the 16th clock cycle has been completed, MS is set high to latch the data into the indexed mode control register.

In addition to single write operations, the PCM1691 also supports multiple write operations, which can be performed by sending the N-bytes (where N ≤ 15) of the 8-bit register data that follow after the first 16-bit register address and register data, while keeping the MC clocks and MS at a low state. Ending a multiple write operation can be accomplished by setting MS to a high state.



(1) X = don't care.

Figure 33. Register Write Operation

TIMING REQUIREMENTS

Figure 34 shows a detailed timing diagram for the three-wire serial control interface. These timing parameters are critical for proper control port operation.

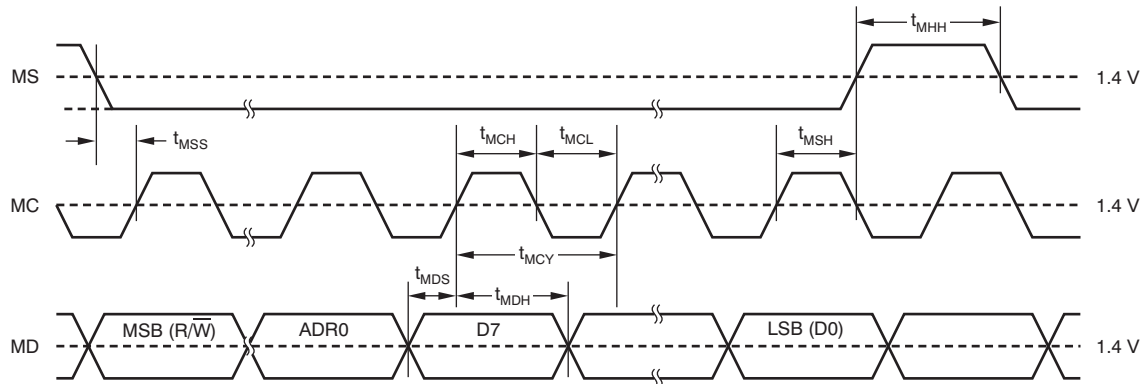


Figure 34. Three-Wire Serial Control Interface Timing

Table 13. Timing Requirements for Figure 34

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-----------|--|-----------|-----|------|
| t_{MCY} | MC pulse cycle time | 100 | | ns |
| t_{MCL} | MC low-level time | 40 | | ns |
| t_{MCH} | MC high-level time | 40 | | ns |
| t_{MHH} | MS high-level time | t_{MCY} | | ns |
| t_{MSS} | MS falling edge to MC rising edge | 30 | | ns |
| t_{MSH} | MS rising edge from MC rising edge for LSB | 15 | | ns |
| t_{MDH} | MD hold time | 15 | | ns |
| t_{MDS} | MD setup time | 15 | | ns |

TWO-WIRE (I²C) SERIAL CONTROL

The PCM1691 supports an I²C-compatible serial bus and data transmission protocol for fast mode configured as a slave device. This protocol is explained in the I²C specification 2.0.

The PCM1691 has a 7-bit slave address, as shown in Figure 35. The first five bits are the most significant bits (MSBs) of the slave address and are factory-preset to '10011'. The next two bits of the address byte are selectable bits that can be set by MS/ADR0/RSV and TEST/ADR1/RSV. A maximum of four PCM1691s can be connected on the same bus at any one time. Each PCM1691 responds when it receives its own slave address.

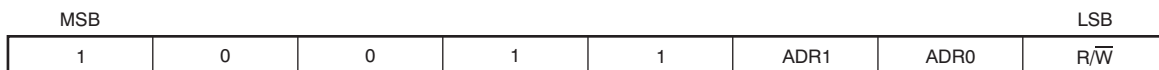
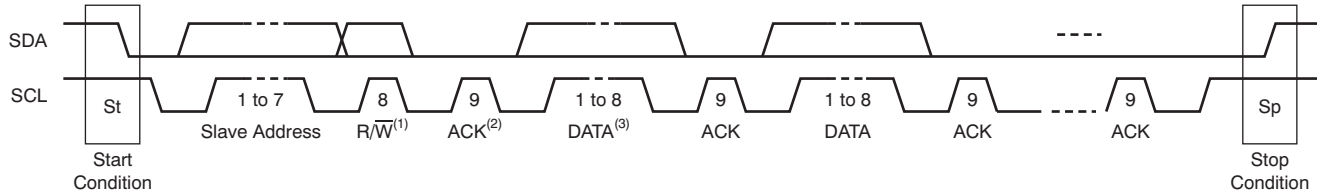


Figure 35. Slave Address

PACKET PROTOCOL

A master device must control the packet protocol, which consists of a start condition, a slave address with the read/write bit, data if a write operation is required, an acknowledgment if a read operation is required, and a stop condition. The PCM1691 supports both slave receiver and transmitter functions. Details about DATA for both write and read operations are described in [Figure 36](#).



- (1) $\overline{R/W}$: Read operation if '1'; write operation otherwise.
- (2) ACK: Acknowledgment of a byte if '0', not Acknowledgment of a byte if '1'.
- (3) DATA: Eight bits (byte); details are described in the [Write Operation](#) and [Read Operation](#) sections.

Figure 36. I²C Packet Control Protocol

WRITE OPERATION

The PCM1691 supports a receiver function. A master device can write to any PCM1691 register using single or multiple accesses. The master sends a PCM1691 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When valid data are received, the index register automatically increments by one. When the register address reaches O, the next value is @. When undefined registers are accessed, the PCM1691 does not send an acknowledgment. [Figure 37](#) illustrates a diagram of the write operation. The register address and write data are in 8-bit, MSB-first format.

| | | | | | | | | | | | | | |
|-------------|----|---------------|----------------|-----|-------------|-----|--------------|-----|--------------|-----|-----|-----|----|
| Transmitter | M | M | M | S | M | S | M | S | M | S | ... | S | M |
| Data Type | St | Slave Address | \overline{W} | ACK | Reg Address | ACK | Write Data 1 | ACK | Write Data 2 | ACK | ... | ACK | Sp |

NOTE: M = Master device, S = Slave device, St = Start condition, \overline{W} = Write, ACK = Acknowledge, and Sp = Stop condition.

Figure 37. Framework for Write Operation

READ OPERATION

A master device can read the registers of the PCM1691. The value of the register address is stored in an indirect index register in advance. The master sends the PCM1691 slave address with a read bit after storing the register address. Then the PCM1691 transfers the data that the index register points to. [Figure 38](#) shows a diagram of the read operation.

| | | | | | | | | | | | | | |
|-------------|----|---------------|----------------|-----|-------------|-----|----|------------------------------|---|-----|-----------|------|----|
| Transmitter | M | M | M | S | M | S | M | M | M | S | S | M | M |
| Data Type | St | Slave Address | \overline{W} | ACK | Reg Address | ACK | Sr | Slave Address ⁽¹⁾ | R | ACK | Read Data | NACK | Sp |

- (1) The slave address after the repeated start condition must be the same as the previous slave address.

NOTE: M = Master device, S = Slave device, St = Start condition, Sr = Repeated start condition, \overline{W} = Write, R = Read, ACK = Acknowledge, NACK = Not acknowledge, and Sp = Stop condition.

Figure 38. Framework for Read Operation

TIMING REQUIREMENTS: SCL AND SDA

A detailed timing diagram for SCL and SDA is shown in [Figure 39](#).

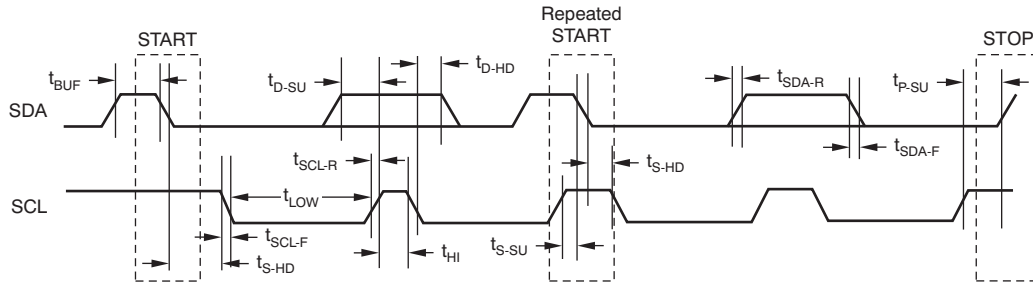


Figure 39. SCL and SDA Control Interface Timing

Table 14. Timing Requirements for [Figure 39](#)

| SYMBOL | PARAMETER | STANDARD MODE | | FAST MODE | | UNIT |
|-------------|---|---------------------|------|----------------------|-----|---------|
| | | MIN | MAX | MIN | MAX | |
| f_{SCL} | SCL clock frequency | | 100 | | 400 | kHz |
| t_{BUF} | Bus free time between STOP and START condition | 4.7 | | 1.3 | | μs |
| t_{LOW} | Low period of the SCL clock | 4.7 | | 1.3 | | μs |
| t_{HI} | High period of the SCL clock | 4.0 | | 0.6 | | μs |
| t_{S-SU} | Setup time for START/Repeated START condition | 4.7 | | 0.6 | | μs |
| t_{S-HD} | Hold time for START/Repeated START condition | 4.0 | | 0.6 | | μs |
| t_{D-SU} | Data setup time | 250 | | 100 | | ns |
| t_{D-HD} | Data hold time | 0 | 3450 | 0 | 900 | ns |
| t_{SCL-R} | Rise time of SCL signal | | 1000 | $20 + 0.1 C_B$ | 300 | ns |
| t_{SCL-F} | Fall time of SCL signal | | 1000 | $20 + 0.1 C_B$ | 300 | ns |
| t_{SDA-R} | Rise time of SDA signal | | 1000 | $20 + 0.1 C_B$ | 300 | ns |
| t_{SDA-F} | Fall time of SDA signal | | 1000 | $20 + 0.1 C_B$ | 300 | ns |
| t_{P-SU} | Setup time for STOP condition | 4.0 | | 0.6 | | μs |
| t_{GW} | Allowable glitch width | | N/A | | 50 | ns |
| C_B | Capacitive load for SDA and SCL line | | 400 | | 100 | pF |
| V_{NH} | Noise margin at high level for each connected device (including hysteresis) | $0.2 \times V_{DD}$ | | $0.2 \times V_{DD}$ | | V |
| V_{NL} | Noise margin at low level for each connected device (including hysteresis) | $0.1 \times V_{DD}$ | | $0.1 \times V_{DD}$ | | V |
| V_{HYS} | Hysteresis of Schmitt trigger input | N/A | | $0.05 \times V_{DD}$ | | V |

CONTROL REGISTER DEFINITIONS (SOFTWARE MODE ONLY)

The PCM1691 has many user-programmable functions that are accessed via control registers, and are programmed through the SPI or I²C serial control port. [Table 15](#) shows the available mode control functions along with reset default conditions and associated register addresses. [Table 16](#) lists the register map.

Table 15. User-Programmable Mode Control Functions

| FUNCTION | RESET DEFAULT | REGISTER | LABEL |
|--------------------------------------|---|----------|------------|
| Mode control register reset | Normal operation | 64 | MRST |
| System reset | Normal operation | 64 | SRST |
| Analog mute function control | Mute disabled | 64 | AMUTE[3:0] |
| Sampling mode selection | Auto | 64 | SRDA[1:0] |
| Power-save mode selection | Power save | 65 | PSMDA |
| Audio interface format selection | I ² S | 65 | FMTDA[3:0] |
| Operation control | Normal operation | 66 | OPEDA[3:0] |
| Digital filter roll-off control | Sharp roll-off | 66 | FLT[3:0] |
| Output phase selection | Normal | 67 | REVDA[8:1] |
| Soft mute control | Mute disabled | 68 | MUTDA[8:1] |
| Zero flag | Not detected | 69 | ZERO[8:1] |
| Digital attenuation mode | 0 dB to –63 dB, 0.5-dB step | 70 | DAMS |
| Digital de-emphasis function control | Disabled | 70 | DEMP[1:0] |
| Zero flag function selection | ZERO1: DIN1 left-channel ZERO2: DIN1 right-channel | 70 | AZRO[1:0] |
| Zero flag polarity selection | High for detection | 70 | ZREV |
| Digital attenuation level setting | 0 dB, no attenuation | 71 to 79 | ATDAx[7:0] |

Table 16. Register Map

| ADR[6:0] | | DATA[7:0] | | | | | | | |
|----------|-----|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 64 | 40 | MRST | SRST | AMUTE3 | AMUTE2 | AMUTE1 | AMUTE0 | SRDA1 | SRDA0 |
| 65 | 41 | PSMDA | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | FMTDA3 | FMTDA2 | FMTDA1 | FMTDA0 |
| 66 | 42 | OPEDA3 | OPEDA2 | OPEDA1 | OPEDA0 | FLT3 | FLT2 | FLT1 | FLT0 |
| 67 | 43 | REVDA8 | REVDA7 | REVDA6 | REVDA5 | REVDA4 | REVDA3 | REVDA2 | REVDA1 |
| 68 | 44 | MUTDA8 | MUTDA7 | MUTDA6 | MUTDA5 | MUTDA4 | MUTDA3 | MUTDA2 | MUTDA1 |
| 69 | 45 | ZERO8 | ZERO7 | ZERO6 | ZERO5 | ZERO4 | ZERO3 | ZERO2 | ZERO1 |
| 70 | 46 | DAMS | RSV ⁽¹⁾ | DEMP1 | DEMP0 | RSV ⁽¹⁾ | AZRO1 | AZRO0 | ZREV |
| 71 | 47 | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ |
| 72 | 48 | ATDA17 | ATDA16 | ATDA15 | ATDA14 | ATDA13 | ATDA12 | ATDA11 | ATDA10 |
| 73 | 49 | ATDA27 | ATDA26 | ATDA25 | ATDA24 | ATDA23 | ATDA22 | ATDA21 | ATDA20 |
| 74 | 4A | ATDA37 | ATDA36 | ATDA35 | ATDA34 | ATDA33 | ATDA32 | ATDA31 | ATDA30 |
| 75 | 4B | ATDA47 | ATDA46 | ATDA45 | ATDA44 | ATDA43 | ATDA42 | ATDA41 | ATDA40 |
| 76 | 4C | ATDA57 | ATDA56 | ATDA55 | ATDA54 | ATDA53 | ATDA52 | ATDA51 | ATDA50 |
| 77 | 4D | ATDA67 | ATDA66 | ATDA65 | ATDA64 | ATDA63 | ATDA62 | ATDA61 | ATDA60 |
| 78 | 4E | ATDA77 | ATDA76 | ATDA75 | ATDA74 | ATDA73 | ATDA72 | ATDA71 | ATDA70 |
| 79 | 4F | ATDA87 | ATDA86 | ATDA85 | ATDA84 | ATDA83 | ATDA82 | ATDA81 | ATDA80 |

(1) RSV must be set to '0'.

REGISTER DEFINITIONS

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|------|------|--------|--------|--------|--------|-------|-------|
| 64 | 40 | MRST | SRST | AMUTE3 | AMUTE2 | AMUTE1 | AMUTE0 | SRDA1 | SRDA0 |

MRST Mode control register reset

This bit sets the mode control register reset to the default value. Pop noise may be generated. Returning the MRST bit to '1' is unnecessary because it is automatically set to '1' after the mode control register is reset.

Default value = 1.

MRST Mode control register reset

| | |
|---|----------------------------|
| 0 | Set default value |
| 1 | Normal operation (default) |

SRST System reset

This bit controls the system reset, which includes the resynchronization between the system clock and sampling clock, and DAC operation restart. The mode control register is not reset and the PCM1691 does not go into a power-down state. Returning the SRST bit to '1' is unnecessary; it is automatically set to '1' after triggering a system reset.

Default value = 1.

SRST System reset

| | |
|---|----------------------------|
| 0 | Resynchronization |
| 1 | Normal operation (default) |

AMUTE[3:0] Analog mute function control

These bits control the enabling/disabling of each source event that triggers the analog mute control circuit.

Default value = 0000.

AMUTE Analog mute function control

| | |
|------|---|
| xxx0 | Disable analog mute control by SCKI halt |
| xxx1 | Enable analog mute control by SCKI halt |
| xx0x | Disable analog mute control by asynchronous detect |
| xx1x | Enable analog mute control by asynchronous detect |
| x0xx | Disable analog mute control by ZERO1 and ZERO2 detect |
| x1xx | Enable analog mute control by ZERO1 and ZERO2 detect |
| 0xxx | Disable analog mute control by DAC disable command |
| 1xxx | Enable analog mute control by DAC disable command |

SRDA[1:0] Sampling mode selection

These bits control the sampling mode of DAC operation. In Auto mode, the sampling mode is automatically set according to multiples between the system clock and sampling clock: single rate for $512 f_S$, $768 f_S$, and $1152 f_S$, dual rate for $256 f_S$ or $384 f_S$, and quad rate for $128 f_S$ and $192 f_S$.

Default value = 00.

SRDA Sampling mode selection

| | |
|----|----------------|
| 00 | Auto (default) |
| 01 | Single rate |
| 10 | Dual rate |
| 11 | Quad rate |

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-------|-----|-----|-----|--------|--------|--------|--------|
| 65 | 41 | PSMDA | RSV | RSV | RSV | FMTDA2 | FMTDA2 | FMTDA1 | FMTDA0 |

PSMDA Power-save mode selection

This bit selects the power-save mode for the OPEDA[3:0] function. When PSMDA = 0, OPEDA[3:0] controls the power-save mode and normal operation. When PSMDA = 1, OPEDA[3:0] controls the DAC disable (not power-save mode) and normal operation.

Default value: 0.

PSMDA Power-save mode selection

| | |
|---|----------------------------------|
| 0 | Power-save enable mode (default) |
| 1 | Power-save disable mode |

RSV Reserved

Reserved; do not use.

FMTDA[3:0] Audio interface format selection

These bits control the audio interface format for DAC operation. Details of the format and any related restrictions with the system clock are described in the [Audio Data Interface Formats and Timing](#) section.

Default value: 0000 (16-/20-/24-/32-bit I²S format).

FMTDA Audio interface format selection

| | |
|------|--|
| 0000 | 16-/20-/24-/32-bit I ² S format (default) |
| 0001 | 16-/20-/24-/32-bit left-justified format |
| 0010 | 24-bit right-justified format |
| 0011 | 16-bit right-justified format |
| 0100 | 24-bit I ² S mode, DSP format |
| 0101 | 24-bit left-justified mode, DSP format |
| 0110 | 24-bit I ² S mode, TDM format |
| 0111 | 24-bit left-justified mode, TDM format |
| 1000 | 24-bit high-speed I ² S mode, TDM format |
| 1001 | 24-bit high-speed left-justified mode, TDM format |
| 101x | Reserved |
| 11xx | Reserved |

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|--------|--------|--------|--------|------|------|------|------|
| 66 | 42 | OPEDA3 | OPEDA2 | OPEDA1 | OPEDA0 | FLT3 | FLT2 | FLT1 | FLT0 |

OPEDA[3:0] Operation control

These bits control the DAC operation mode. In operation disable mode, the DAC output is cut off from DIN and the internal DAC data are reset. If PSM DA = 1, the DAC output is forced into VCOM. If PSM DA = 0, the DAC output is forced into AGND and the DAC goes into a power-down state. For normal operating mode, these bits must be '0'. The serial mode control is effective during operation disable mode.

Default value: 0000.

OPEDA Operation control

| | |
|------|---|
| xxx0 | DAC1/2 normal operation |
| xxx1 | DAC1/2 operation disable with or without power save |
| xx0x | DAC3/4 normal operation |
| xx1x | DAC3/4 operation disable with or without power save |
| x0xx | DAC5/6 normal operation |
| x1xx | DAC5/6 operation disable with or without power save |
| 0xxx | DAC7/8 normal operation |
| 1xxx | DAC7/8 operation disable with or without power save |

FLT[3:0] Digital filter roll-off control

These bits allow users to select the digital filter roll-off that is best suited to their applications. Sharp and slow filter roll-off selections are available. The filter responses for these selections are shown in the [Typical Characteristics](#) sections of this data sheet.

Default value: 0000.

FLT Digital filter roll-off control

| | |
|------|-----------------------|
| xxx0 | DAC1/2 sharp roll-off |
| xxx1 | DAC1/2 slow roll-off |
| xx0x | DAC3/4 sharp roll-off |
| xx1x | DAC3/4 slow roll-off |
| x0xx | DAC5/6 sharp roll-off |
| x1xx | DAC5/6 slow roll-off |
| 0xxx | DAC7/8 sharp roll-off |
| 1xxx | DAC7/8 slow roll-off |

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| 67 | 43 | REVDA8 | REVDA7 | REVDA6 | REVDA5 | REVDA4 | REVDA3 | REVDA2 | REVDA1 |

REVDA[8:1] Output phase selection

These bits are used to control the phase of the DAC analog signal outputs.

Default value: 0000 0000.

REVDA Output phase selection

| | |
|-----------|----------------------|
| xxxx xxx0 | DAC1 normal output |
| xxxx xxx1 | DAC1 inverted output |
| xxxx xx0x | DAC2 normal output |
| xxxx xx1x | DAC2 inverted output |
| xxxx x0xx | DAC3 normal output |
| xxxx x1xx | DAC3 inverted output |
| xxxx 0xxx | DAC4 normal output |
| xxxx 1xxx | DAC4 inverted output |
| xxx0 xxxx | DAC5 normal output |
| xxx1 xxxx | DAC5 inverted output |
| xx0x xxxx | DAC6 normal output |
| xx1x xxxx | DAC6 inverted output |
| x0xx xxxx | DAC7 normal output |
| x1xx xxxx | DAC7 inverted output |
| 0xxx xxxx | DAC8 normal output |
| 1xxx xxxx | DAC8 inverted output |

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| 68 | 44 | MUTDA8 | MUTDA7 | MUTDA6 | MUTDA5 | MUTDA4 | MUTDA3 | MUTDA2 | MUTDA1 |

MUTDA[8:1] Soft Mute control

These bits are used to enable or disable the Soft Mute function for the corresponding DAC outputs, VOUTx. The Soft Mute function is incorporated into the digital attenuators. When mute is disabled (MUTDA[8:1] = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTDA[8:1] = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation. By setting MUTDA[8:1] = 0, the attenuator is increased to the last attenuation level in the same manner as it is for decreasing levels. This configuration reduces *pop and zipper noise* during muting of the DAC output. This Soft Mute control uses the same resource of digital attenuation level setting. Mute control has priority over the digital attenuation level setting.

Default value: 0000 0000.

| MUTDA | Soft Mute control |
|-----------|--------------------|
| xxxx xxx0 | DAC1 Mute disabled |
| xxxx xxx1 | DAC1 Mute enabled |
| xxxx xx0x | DAC2 Mute disabled |
| xxxx xx1x | DAC2 Mute enabled |
| xxxx x0xx | DAC3 Mute disabled |
| xxxx x1xx | DAC3 Mute enabled |
| xxxx 0xxx | DAC4 Mute disabled |
| xxxx 1xxx | DAC4 Mute enabled |
| xxx0 xxxx | DAC5 Mute disabled |
| xxx1 xxxx | DAC5 Mute enabled |
| xx0x xxxx | DAC6 Mute disabled |
| xx1x xxxx | DAC6 Mute enabled |
| x0xx xxxx | DAC7 Mute disabled |
| x1xx xxxx | DAC7 Mute enabled |
| 0xxx xxxx | DAC8 Mute disabled |
| 1xxx xxxx | DAC8 Mute enabled |

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| 69 | 45 | ZERO8 | ZERO7 | ZERO6 | ZERO5 | ZERO4 | ZERO3 | ZERO2 | ZERO1 |

ZERO[8:1] Zero flag (read-only)

These bits indicate the present status of the zero detect circuit for each DAC channel; these bits are read-only.

| ZERO | Zero flag |
|-------------|------------------------------|
| xxxx xxx0 | DAC1 zero input not detected |
| xxxx xxx1 | DAC1 zero input detected |
| xxxx xx0x | DAC2 zero input not detected |
| xxxx xx1x | DAC2 zero input detected |
| xxxx x0xx | DAC3 zero input not detected |
| xxxx x1xx | DAC3 zero input detected |
| xxxx 0xxx | DAC4 zero input not detected |
| xxxx 1xxx | DAC4 zero input detected |
| xxx0 xxxx | DAC5 zero input not detected |
| xxx1 xxxx | DAC5 zero input detected |
| xx0x xxxx | DAC6 zero input not detected |
| xx1x xxxx | DAC6 zero input detected |
| x0xx xxxx | DAC7 zero input not detected |
| x1xx xxxx | DAC7 zero input detected |
| 0xxx xxxx | DAC8 zero input not detected |
| 1xxx xxxx | DAC8 zero input detected |

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|------|-----|-------|-------|-----|-------|-------|------|
| 70 | 46 | DAMS | RSV | DEMP1 | DEMP0 | RSV | AZRO1 | AZRO0 | ZREV |

DAMS Digital attenuation mode

This bit selects the attenuation mode.

Default value: 0.

DAMS Digital attenuation mode

- | | |
|---|---|
| 0 | Fine step: 0.5-dB step for 0 dB to –63 dB range (default) |
| 1 | Wide range: 1-dB step for 0 dB to –100 dB range |

RSV Reserved

Reserved; do not use.

DEMP[1:0] Digital de-emphasis function/sampling rate control

These bits are used to disable and enable the various sampling frequencies of the digital de-emphasis function.

Default value: 00.

DEMP Digital de-emphasis function/sampling rate control

- | | |
|----|-------------------|
| 00 | Disable (default) |
| 01 | 48 kHz enable |
| 10 | 44.1 kHz enable |
| 11 | 32 kHz enable |

AZRO[1:0] Zero flag channel combination selection

These bits are used to select the zero flag channel combination for ZERO1 and ZERO2.

If the analog mute function control by ZERO flags is used, AZRO[1:0] should not be set '00'; otherwise, the analog mute works even if the data of DIN2-4 are not zero.

Default value: 00.

AZRO Zero flag combination selection

- | | |
|----|--|
| 00 | Combination A: ZERO1 = DIN1 left channel, ZERO2 = DIN1 right channel (default) |
| 01 | Combination B: ZERO1 = DIN1-4, ZERO2 = DIN1-4 |
| 10 | Combination C: ZERO1 = DIN4, ZERO2 = DIN1-3 |
| 11 | Combination D: ZERO1 = DIN1, ZERO2 = DIN2-4 |

ZREV Zero flag polarity selection

This bit controls the polarity of the zero flag pin.

Default value: 0.

ZREV Zero flag polarity selection

- | | |
|---|--------------------------------|
| 0 | High for zero detect (default) |
| 1 | Low for zero detect |

| DEC | HEX | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| 71 | 47 | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 72 | 48 | ATDA17 | ATDA16 | ATDA15 | ATDA14 | ATDA13 | ATDA12 | ATDA11 | ATDA10 |
| 73 | 49 | ATDA27 | ATDA26 | ATDA25 | ATDA24 | ATDA23 | ATDA22 | ATDA21 | ATDA20 |
| 74 | 4A | ATDA37 | ATDA36 | ATDA35 | ATDA34 | ATDA33 | ATDA32 | ATDA31 | ATDA30 |
| 75 | 4B | ATDA47 | ATDA46 | ATDA45 | ATDA44 | ATDA43 | ATDA42 | ATDA41 | ATDA40 |
| 76 | 4C | ATDA57 | ATDA56 | ATDA55 | ATDA54 | ATDA53 | ATDA52 | ATDA51 | ATDA50 |
| 77 | 4D | ATDA67 | ATDA66 | ATDA65 | ATDA64 | ATDA63 | ATDA62 | ATDA61 | ATDA60 |
| 78 | 4E | ATDA77 | ATDA76 | ATDA75 | ATDA74 | ATDA73 | ATDA72 | ATDA71 | ATDA70 |
| 79 | 4F | ATDA87 | ATDA86 | ATDA85 | ATDA84 | ATDA83 | ATDA82 | ATDA81 | ATDA80 |

RSV Reserved

Reserved; do not use.

ATDAx[7:0] Digital attenuation level setting

Where $x = 1$ to 8, corresponding to the DAC output ($VOUT_x$).

Each DAC output ($VOUT_1$ through $VOUT_8$) has a digital attenuation function. The attenuation level can be set from 0 dB to R dB, in S-dB steps. Changes in attenuator levels are made by incrementing or decrementing one step (S dB) for every $8/f_s$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute). R (range) and S (step) is -63 and 0.5 for DAMS = 0, and -100 and 1.0 for DAMS = 1, respectively. The DAMS bit is defined in register 70 (46h). [Table 17](#) shows attenuation levels for various settings.

The attenuation level for each channel can be set individually using the following formula:

$$\text{Attenuation level (dB)} = S \times (\text{ATDAx}[7:0]_{\text{DEC}} - 255)$$

where $\text{ATDAx}[7:0]_{\text{DEC}} = 0$ through 255.

For $\text{ATDAx}[7:0]_{\text{DEC}} = 0$ through 128 with DAMS = 0, or 0 through 154 with DAMS = 1, attenuation is set to infinite attenuation (mute).

Default value: 1111 1111.

Table 17. Attenuation Levels for Various Settings

| ATDAx[7:0] | | ATTENUATION LEVEL SETTING | |
|------------|---------|--------------------------------|--------------------------------|
| BINARY | DECIMAL | DAMS = 0 | DAMS = 1 |
| 1111 1111 | 255 | 0 dB, no attenuation (default) | 0 dB, no attenuation (default) |
| 1111 1110 | 254 | -0.5 dB | -1 dB |
| 1111 1101 | 253 | -1.0 dB | -2 dB |
| ... | ... | ... | ... |
| 1001 1100 | 156 | -45.9 dB | -99 dB |
| 1001 1011 | 155 | -50.0 dB | -100 dB |
| 1001 1010 | 154 | -50.5 dB | Mute |
| ... | ... | ... | ... |
| 1000 0010 | 130 | -62.5 dB | Mute |
| 1000 0001 | 129 | -63.0 dB | Mute |
| 0000 0000 | 128 | Mute | Mute |
| ... | ... | ... | ... |
| 0000 0000 | 0 | Mute | Mute |

APPLICATION INFORMATION

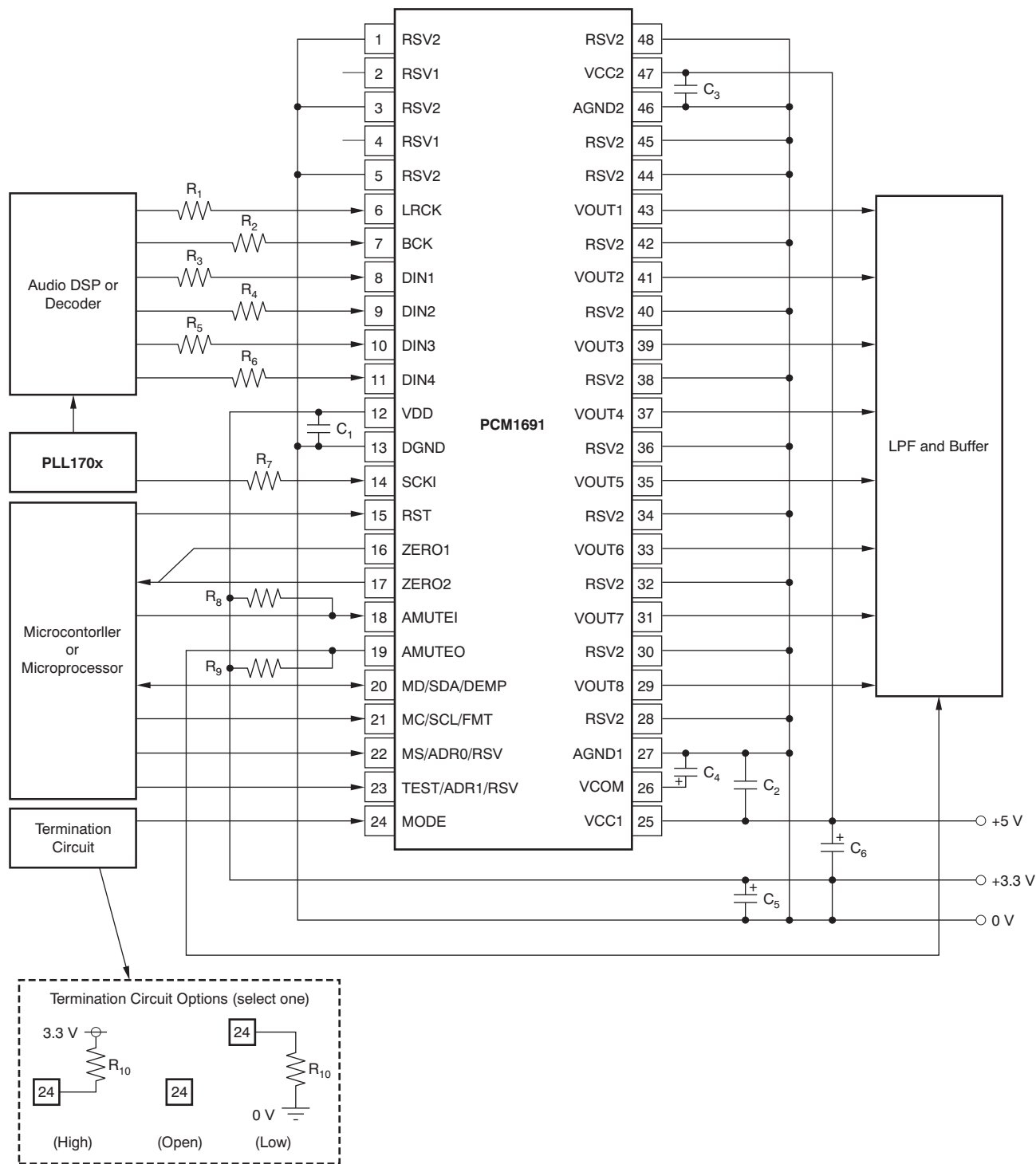
CONNECTION DIAGRAMS

A basic connection diagram is shown in [Figure 40](#), with the necessary power-supply bypassing and decoupling components. Texas Instruments' [PLL170X](#) is used to generate the system clock input at SCKI, as well as to generate the clock for the audio signal processor. The use of series resistors (22 Ω to 100 Ω) are recommended for SCKI, LRCK, BCK, DIN1, DIN2, DIN3, and DIN4 for electromagnetic interference (EMI) reduction.

POWER SUPPLY AND GROUNDING

The PCM1691 requires +5 V for the analog supply and +3.3 V for the digital supply. The +5-V supply is used to power the DAC analog and output filter circuitry, and the +3.3-V supply is used to power the digital filter and serial interface circuitry. For best performance, it is recommended to use a linear regulator (such as the [REG102-5/33](#) or [REG103-5/33](#)) with the +5-V and +3.3-V supplies.

Five capacitors are required for supply bypassing, as shown in [Figure 40](#). These capacitors should be located as close as possible to the PCM1691 package. The 10- μ F capacitors are aluminum electrolytic, while the three 1- μ F capacitors are ceramic.



NOTE: C₁ through C₃ are 1-μF ceramic capacitors. C₄ through C₆ are 10-μF electrolytic capacitors. R₁ through R₇ are 22-Ω to 100-Ω resistors. R₈ and R₉ are resistors appropriate for pull-up. R₁₀ is less than 10 kΩ.

Figure 40. Basic Connection Diagram

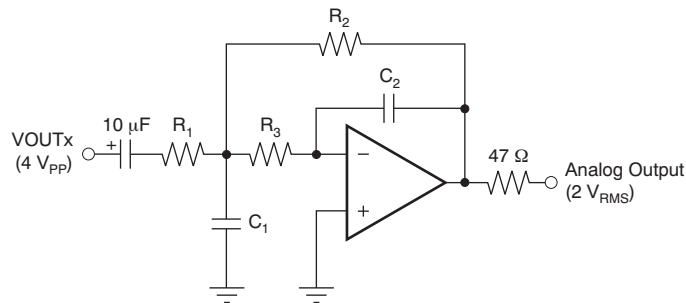
LOW-PASS FILTER AND SINGLE-ENDED BUFFER FOR DAC OUTPUTS

$\Delta\Sigma$ DACs use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_s/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This filtering is accomplished by a combination of on-chip and external low-pass filters.

Figure 41 and Figure 42 show the recommended external inverting buffer with low-pass active filter circuits for $2 V_{RMS}$ output with a dc block capacitor, and for $2 V_{RMS}$ output without dc block capacitor by using VCOM. These circuits are second-order Butterworth filters using a multiple feedback (MFB) circuit arrangement that reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter designs, please refer to Applications Bulletin SBAA055, *Dynamic Performance Testing of Digital Audio D/A Converters*, available from the TI web site (www.ti.com) or your local Texas Instruments' sales office.

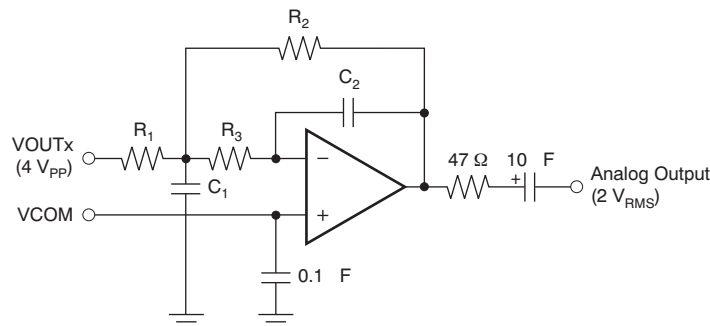
Figure 43 and Figure 44 show the recommended external noninverting buffer with low-pass active filter circuit for $2 V_{RMS}$ output with dc block capacitor, and $1.4V_{RMS}$ output without dc block capacitor using a 5V single supply.

Because the overall system performance is defined by the quality of the DACs and the associated analog output circuitry, high-quality audio op amps are recommended for the active filters. Texas Instruments' OPA2134 and NE5532A dual op amps are shown in Figure 41 Figure 42, and Figure 43. The OPA2353, dual op amp is shown in Figure 44. These op amps are all recommended for use with the PCM1691.



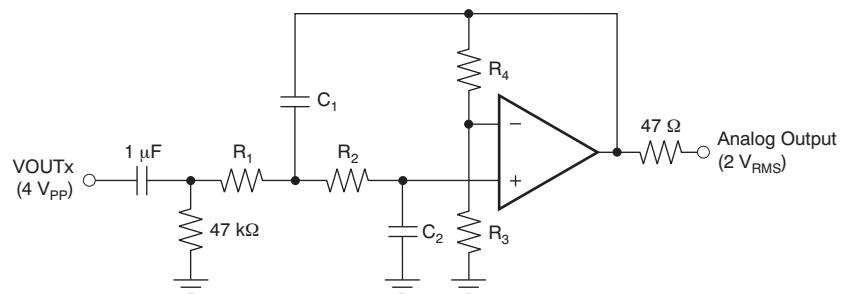
NOTE: Amplifier is an NE5532A x 1/2 or OPA2134 x 1/2; $R_1 = 5.1 \text{ k}\Omega$; $R_2 = 7.5 \text{ k}\Omega$; $R_3 = 470 \Omega$; $C_1 = 4700 \text{ pF}$; $C_2 = 470 \text{ pF}$; Gain = 1.47; $f_{-3 \text{ dB}} = 55 \text{ kHz}$.

Figure 41. Typical Post-LPF and Buffer ($2 V_{RMS}$ Output) for Inverting Output



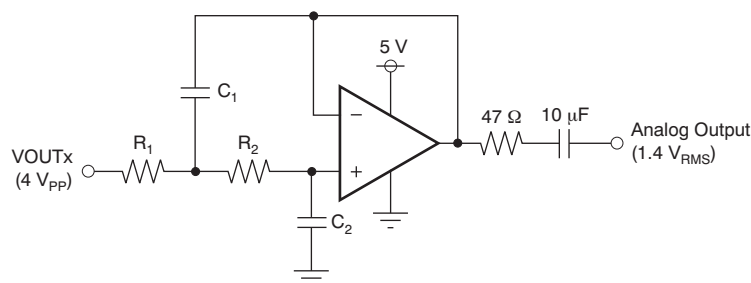
NOTE: Amplifier is an NE5532A x 1/2 or OPA2134 x 1/2; $R_1 = 7.5 \text{ k}\Omega$; $R_2 = 11 \text{ k}\Omega$; $R_3 = 750 \Omega$; $C_1 = 3300 \text{ pF}$; $C_2 = 330 \text{ pF}$; Gain = 1.47; $f_{-3 \text{ dB}} = 53 \text{ kHz}$.

Figure 42. Capless Post-LPF and Buffer Using VCOM ($2 V_{RMS}$ Output) for Inverting Output



NOTE: Amplifier is an NE5532A x 1/2 or OPA2134 x1/2; $R_1 = 2.2 \text{ k}\Omega$; $R_2 = 9.1 \text{ k}\Omega$; $R_3 = 4.7 \text{ k}\Omega$; $R_4 = 2.2 \text{ k}\Omega$; $C_1 = 1000 \text{ pF}$; $C_2 = 470 \text{ pF}$; Gain = 1.47; $f_{-3 \text{ dB}} = 52 \text{ kHz}$.

Figure 43. Typical Post-LPF and Buffer (2 V_{RMS} Output) for Noninverting Output



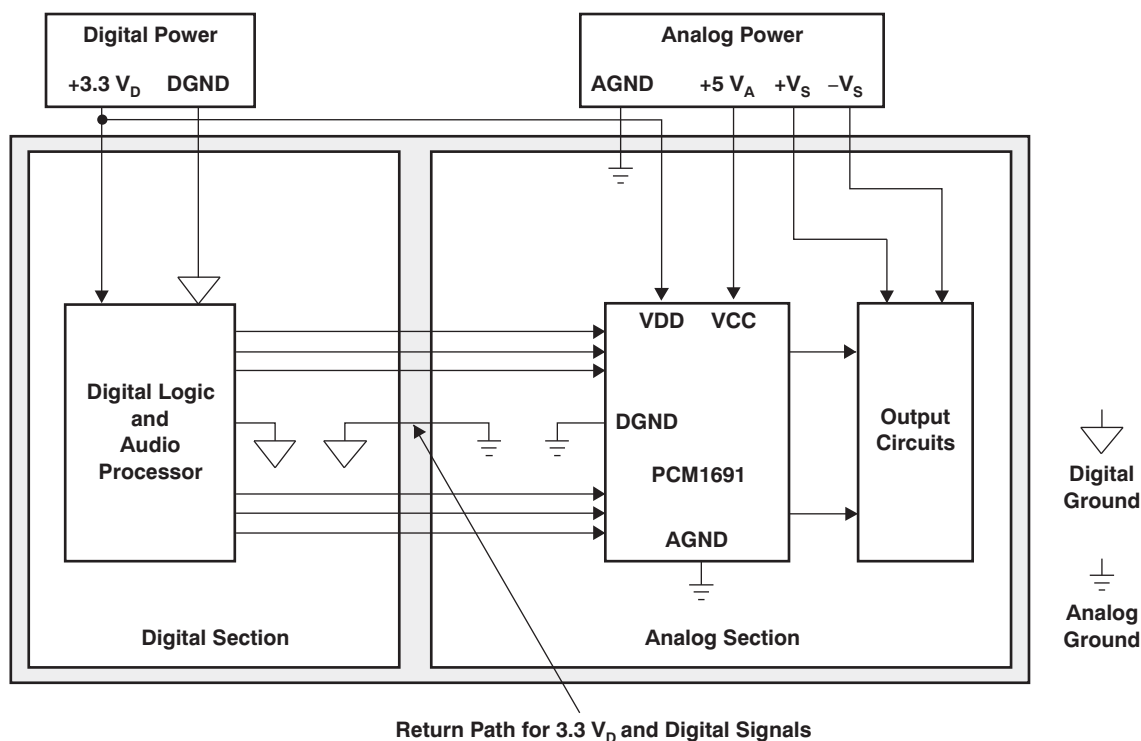
NOTE: Amplifier is an OPA2353 x 1/2; $R_1 = 2.2 \text{ k}\Omega$; $R_2 = 6.8 \text{ k}\Omega$; $C_1 = 1000 \text{ pF}$; $C_2 = 470 \text{ pF}$; Gain = 1.00; $f_{-3 \text{ dB}} = 52 \text{ kHz}$.

Figure 44. Capless Post-LPF and Buffer Using 5-V Single Supply (1.4 V_{RMS} Output) for Noninverting Output

PCB LAYOUT GUIDELINES

A typical printed circuit board (PCB) layout for the PCM1691 is shown in Figure 45. A ground plane is recommended, with the analog and digital sections isolated from one another through a split or cut in the circuit board. The PCM1691 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This configuration prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1691.



Return Path for 3.3 V_D and Digital Signals

Figure 45. Recommended PCB Layout

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| PCM1691DCA | ACTIVE | HTSSOP | DCA | 48 | 40 | Green (RoHS & no Sb/Br) | Cu NiPdAu | Level-3-260C-168 HR |
| PCM1691DCAG4 | ACTIVE | HTSSOP | DCA | 48 | 40 | Green (RoHS & no Sb/Br) | Cu NiPdAu | Level-3-260C-168 HR |
| PCM1691DCAR | ACTIVE | HTSSOP | DCA | 48 | 2000 | Green (RoHS & no Sb/Br) | Cu NiPdAu | Level-3-260C-168 HR |
| PCM1691DCARG4 | ACTIVE | HTSSOP | DCA | 48 | 2000 | Green (RoHS & no Sb/Br) | Cu NiPdAu | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

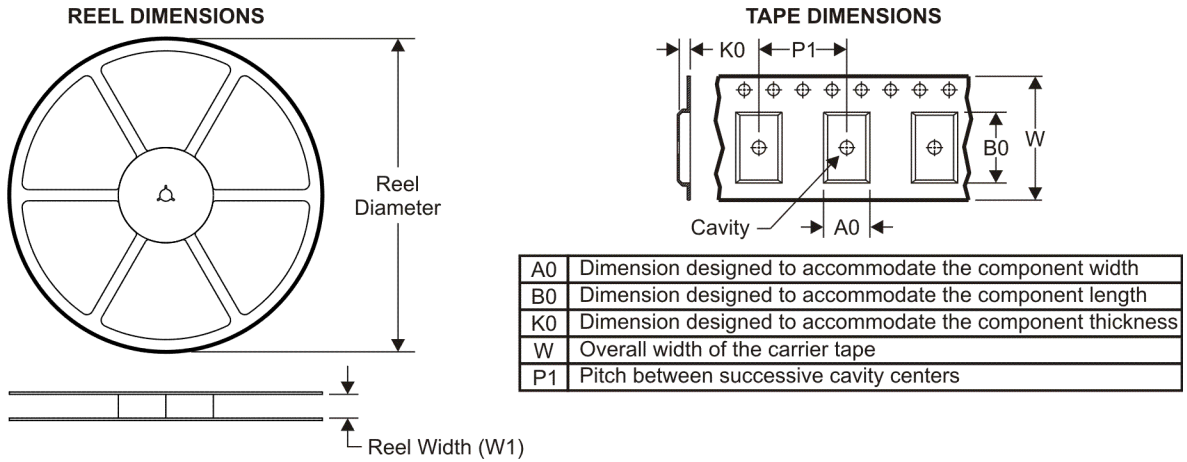
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCM1691DCAR | HTSSOP | DCA | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

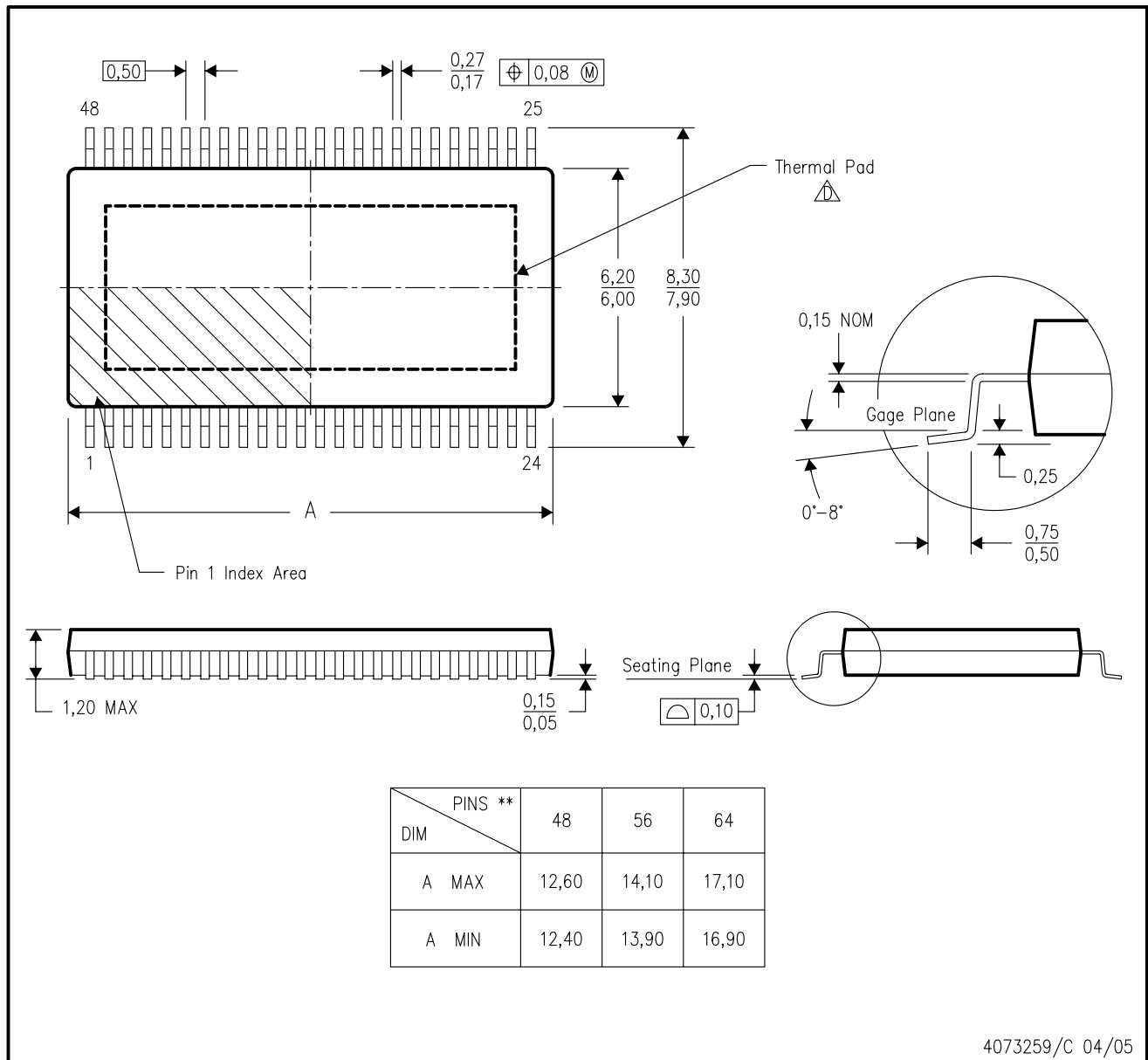
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM1691DCAR | HTSSOP | DCA | 48 | 2000 | 346.0 | 346.0 | 41.0 |

MECHANICAL DATA

DCA (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - △ This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MO-153

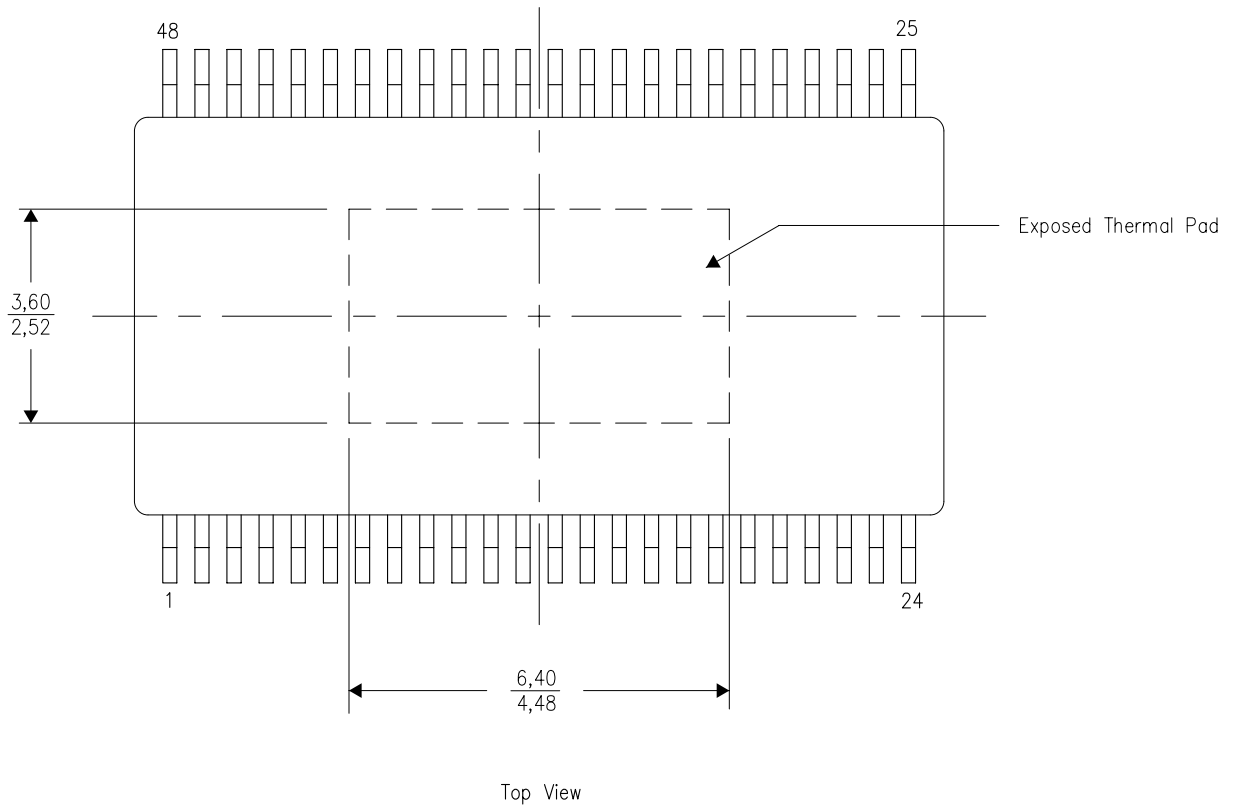
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

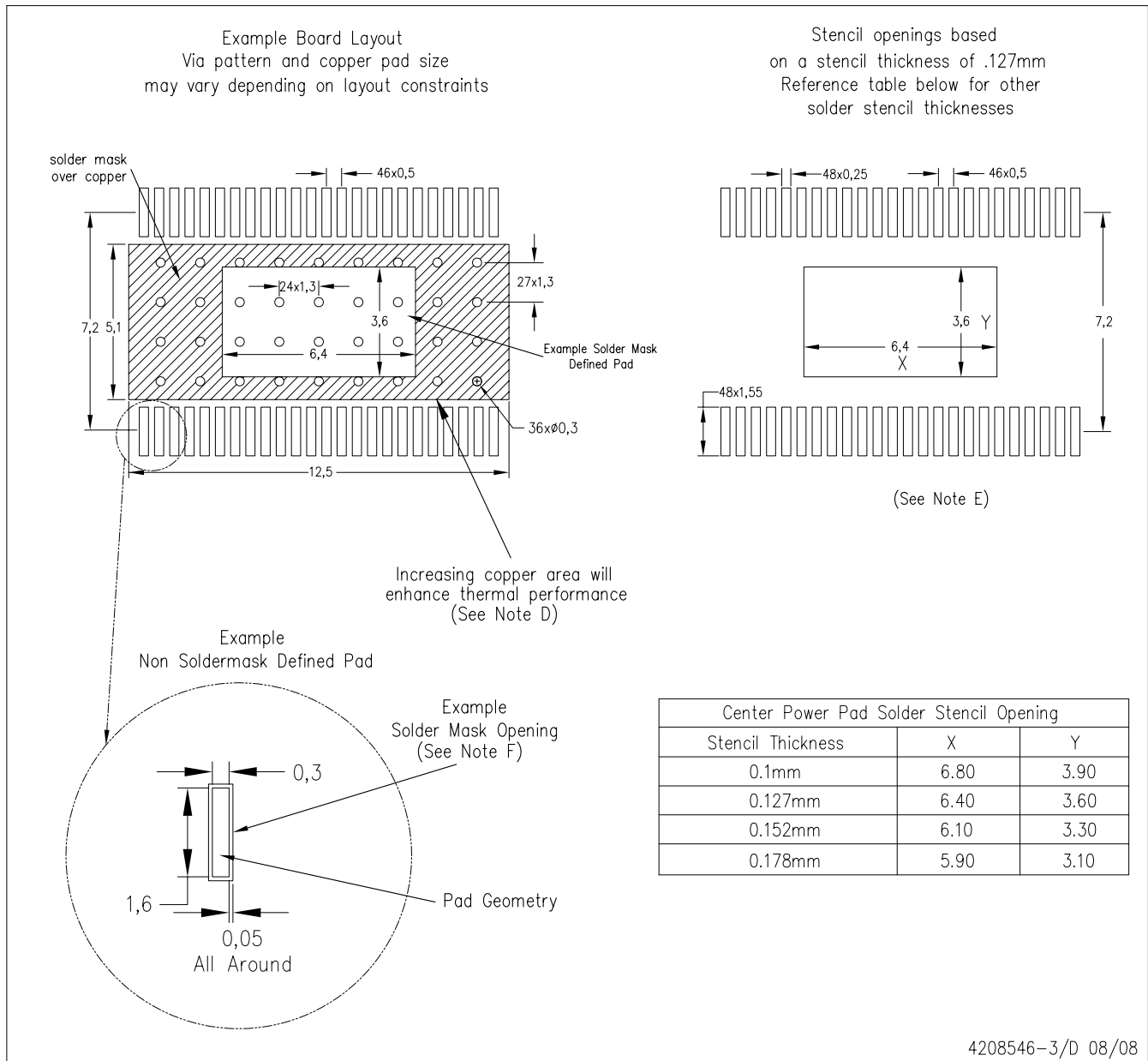
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DCA (R-PDSO-G48) PowerPAD™



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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